Designing PCB Footprint for EPC eGaN® FETs and ICs

How to Design eGaN FET or IC PCB footprint

EPC's wafer level chip-scale packaging such as the Land Grid Array (LGA) and Ball Grid Array (BGA) packages shown in figure 1, has enabled a new level of performance in power conversion. Many of these parts use a fine pitch down to 400 µm which means a proper PCB footprint design is essential for consistent and reliable assembly of the GaN device. Here are the guidelines of designing a correct footprint for any EPC part working from the datasheet.

The purpose of this How2AppNote is to provide the information needed to create a PCB layout footprint for the eGaN FET using the solder mask opening and stencil recommendation provided in the datasheet. This will be done using as examples the EPC2016C and EPC2045 for an LGA and BGA format respectively. The layers involved are the copper immediately beneath the device, soldermask opening, proper silk-screen demarcation, and solder paste.

EPC recommends the use of a Solder Mask Defined (SMD) pad over a Non-Solder Mask Defined (NSMD) pad.

• A SMD footprint yields lower inductance and improves alignment during reflow.

• A NSMD footprint has a higher probability of die misalignment during reflow, which can reduce the effective copper contact area thereby degrading the solder joint and current carrying capability of the device.

Copper pad and soldermask design

In each EPC part datasheet you will find a complete SMD land pattern which defines the solder mask design. What is not defined is the copper pad. Proper SMD pad design requires that the copper pad be physically larger in both x and y directions including manufacturing registration tolerances which will account for any mis-alignment between the solder mask and the copper layers. *EPC recommends a minimum of ±2mils or ±50 µm registration tolerance when using its parts.*

For solder mask thickness EPC recommends a maximum 25 µm.

The recommended soldermask opening may be adjusted by the PCB manufacturer ONLY to adjust for their specific process, but the end result should be the same as recommended in the datasheet.

Tables showing the recommended copper expansion to add can be found on the following pages.

EPC2016C LGA Example:

- Datasheet shows a LGA land pad design with a 1362 µm x 180 µm pad.
- A ±45 µm registration tolerance = 90 µm total adder.
- Copper pad design = 1453 x 270 µm minimum.

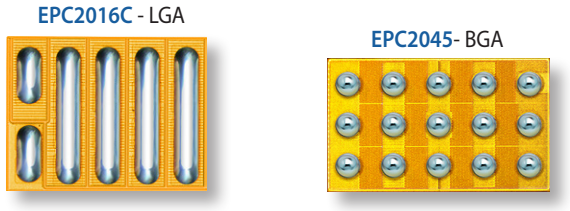


Figure 1. Examples of eGaN FETs in LGA (EPC2016C shown) and BGA (EPC2045 shown) packages

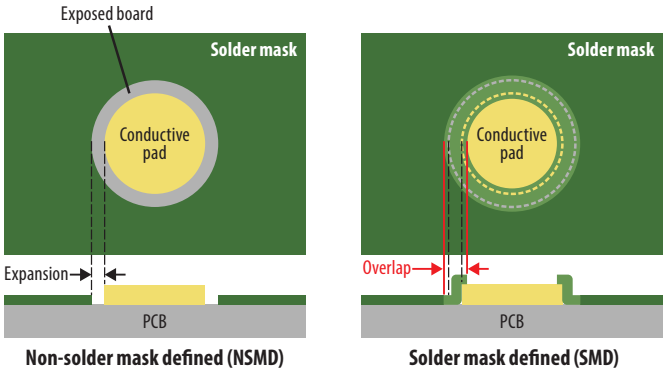


Figure 2. Land Pad comparison: NSMD (Not recommended) vs SMD (Recommended)

EPC2045 BGA Example:

- Datasheet shows a BGA land pad design with a 230 µm diameter.
- A ±50 µm registration tolerance = 100 µm total adder.
- Copper pad diameter = 230 + 100 = 330 µm minimum.
- Copper pads on the same node can be unified.

Open Silkscreen Design

The silkscreen design for EPC devices serves two purposes; 1) Indicates where the die is to be located and orientated, 2) Registration location for the die thus requiring silkscreen layer to copper layer registration tolerance recommendations.

The EPC recommended silkscreen design should include:

- 4 corner registration marks outlining the part shape.
- Lines drawn with open narrow dash.
- Unique Pin one identifier.

See figures 3 & 4 for examples of the recommended silkscreen pattern design.

A solid line rectangle surrounding the part, thus preventing flux from flowing away from the die during the reflow process, can create a flux dam and trap flux under the part. The washing process used to remove the flux and clean the PCB may also not completely clean under the EPC device increasing the likelihood of dendrite formation [AN009]

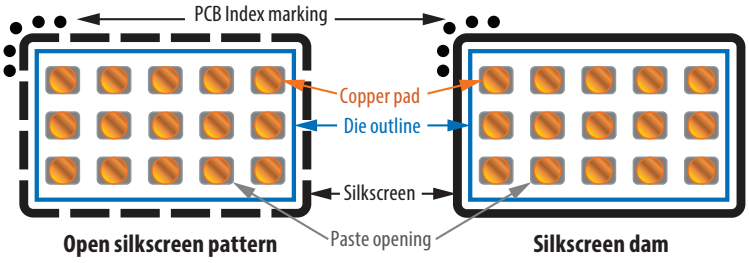


Figure 3. Pad design with silkscreen comparison Open (Recommended), Dam (Not recommended)

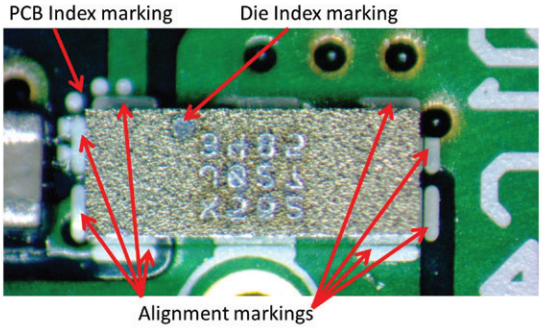


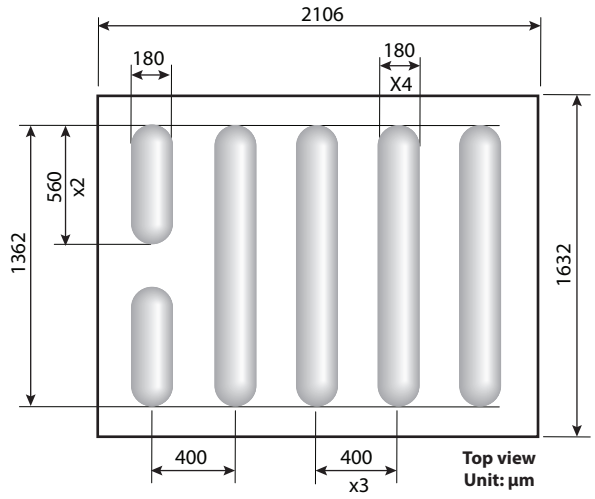
Figure 4. Example of proper silkscreen design

Table 1: Recommended Copper Expansion for LGA Type Devices

Bump Type	Bump Composition	Device Type	Bar Width Post Reflow	Minimum Pitch Different Nodes (µm)	Datasheet Solder Mask Opening Width Size (µm)	Add for Copper Pad (µm)	Copper Pad Size Width (µm)	Copper Pad Size Length (µm)
LGA	97.5Sn / 2.5%Ag	EPC8XXX	200	400	190	80	270	DS solder mask opening + 80 µm
LGA	97.5Sn / 2.5%Ag	EPC2XXX	200	400	180	90	270	DS solder mask opening + 95 µm
LGA	97.5Sn / 2.5%Ag	EPC2XXX	250	600	230	100	330	DS solder mask opening + 70 µm

EPC2016C LGA Example:

Follow the solder mask opening size recommendations in the datasheet. Solder mask opening view:



Solder mask thickness recommendation is 25 µm (1mil) or less

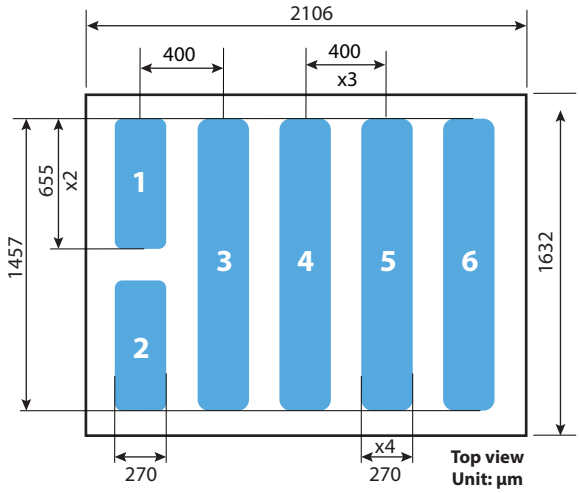
For information only:

The opening size was calculated by looking at the solder bar size and reducing by 10 µm per side. The exception is the EPC8XXX family that has a solder mask opening that was calculated by reducing 5 µm per side.

EPC layouts frequently use 130 µm spacing between copper bars. This will violate the 150 µm minimum spacing design rule that is commonly used by PCB manufacturers. This can be overcome by starting with a thinner copper layer using the 130 µm spacing and then plating up to the final thickness.

EPC2016C Copper Landing Pads

Per table 1, for a solder mask opening width of 180 µm, the copper landing pad should be expanded by 90 µm to result in a total of 270 µm. Similarly, for a solder mask opening length of 1362 µm, the copper landing pad should be expanded by 95 µm to result in a total of 1457 µm. The minimum copper spacing should be 130 µm between different electrical nodes. Copper landing pad sizes shown in figure below:

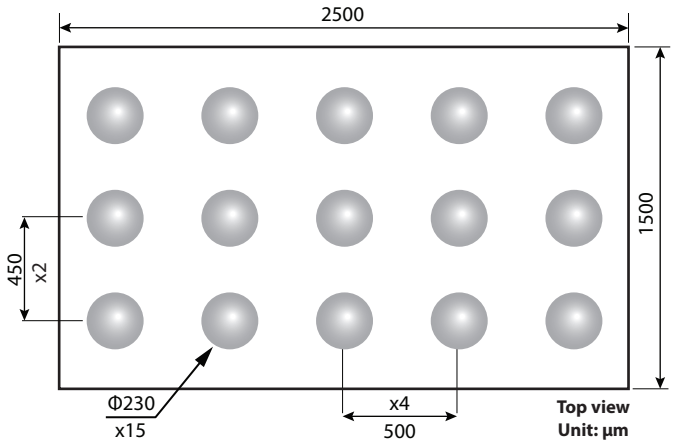


Add Table 2: Recommended Copper Expansion for BGA Type Devices

Bump Type	Bump Composition	Device Type	Nominal Ball Size Before Reflow (µm)	Minimum Pitch Different Nodes (µm)	Nominal Ball Size Post Reflow (µm)	Datasheet Solder Mask Opening Size (µm)	Add for Copper Pad (µm)	Copper Pad Size (µm) Same Nodes will be Joined in Single Bar
BGA	SAC405	Half Bridge	200	400	208	200	70	270
BGA	SAC405	2x2, 2x3, 3x3	200	450	208	200	100	300
BGA	SAC405	All	250	450	264	230	90	320
BGA	SAC405	All	350	1000	369	330	100	430

EPC2045 BGA Example:

Follow the solder mask opening size recommendations in the datasheet. Solder mask opening view:



Solder mask thickness recommendation is 25 µm (1mil) or less.

For information only :

The minimum opening size for the nominal 200 µm BGA does not follow the sizing of the 250 µm and 350 µm balls. The 200 µm ball solder mask opening size is 200 µm, +20 µm /-10 µm. 190 µm minimum opening size to avoid SMD opening issues.

EPC layouts frequently use 130 µm spacing between copper bars. This will violate the 150 µm minimum spacing design rule that is commonly used by PCB manufacturers. This can be overcome by starting with a thinner copper layer using the 130 µm spacing and then plating up to the final thickness.

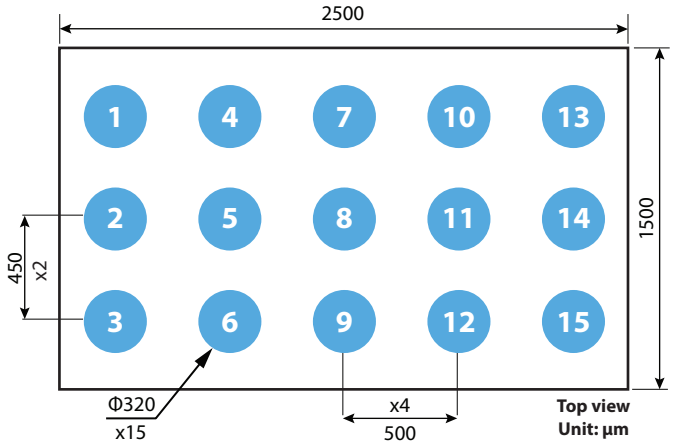
Conclusion

This *How2AppNote* shows the design steps and the additional important considerations for a successful design of an EPC PCB footprint. It will result in a high yield and reliable assembly process when working with voltages 5 V and upwards. For more information on assembly, see application note AN009.

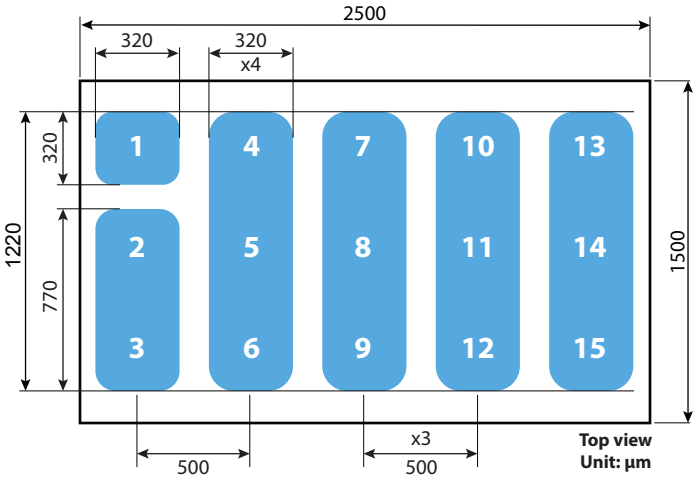
Stencil recommendations can be found for each device in their respective datasheet.

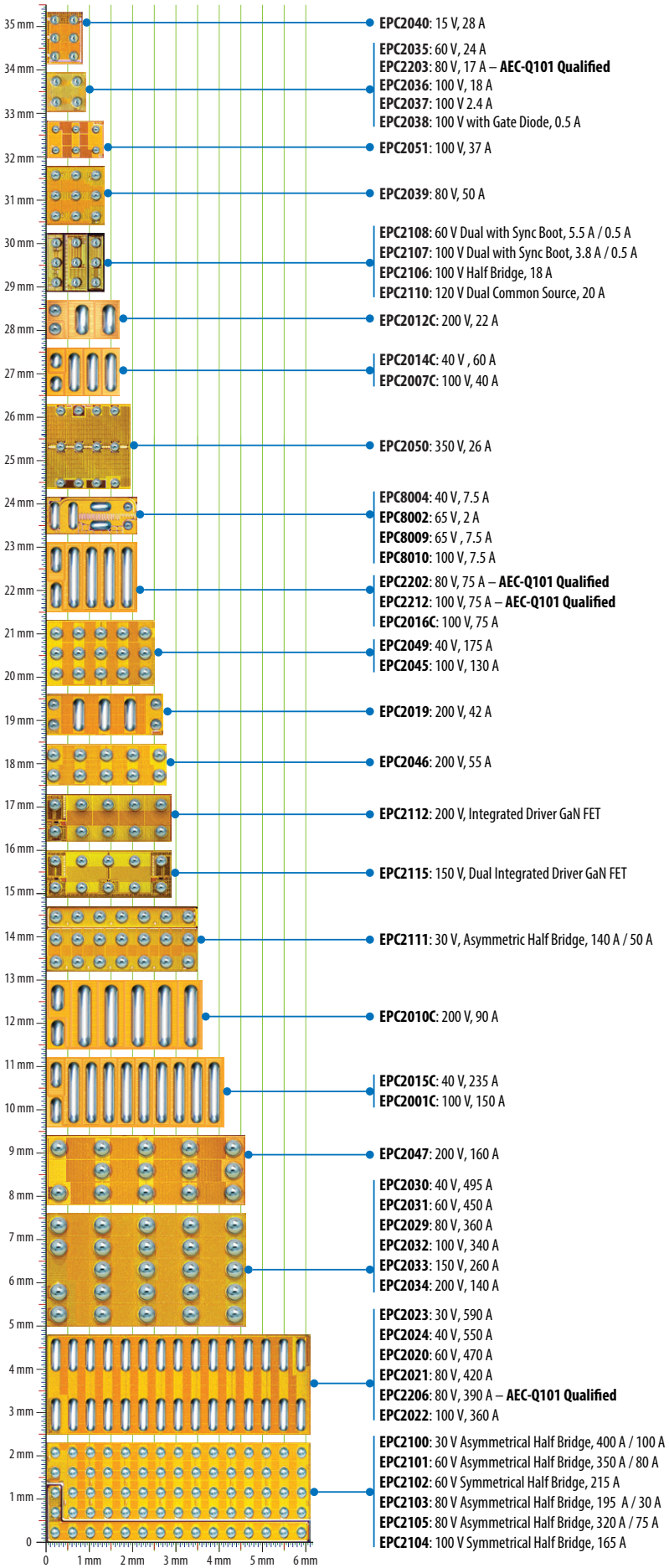
EPC2045 Copper Landing Pads

Per table 2, for a solder mask opening of 230 µm, the copper landing pad should be expanded by 90 µm to result in a total of 320 µm. Copper landing pad sizes shown in figure below:



The minimum copper spacing should be 130 µm between different electrical nodes. Bumps on the same electrical node may be connected together using a single bar design with multiple solder mask openings. Bars can be expanded up to 370 µm while still observing the 130 µm minimum spacing recommendation. Connected node copper landing pad sizes shown in figure below:





EPC2040: 15 V, 28 A

EPC2035: 60 V, 24 A
EPC2203: 80 V, 17 A – **AEC-Q101 Qualified**
EPC2036: 100 V, 18 A
EPC2037: 100 V 2.4 A
EPC2038: 100 V with Gate Diode, 0.5 A

EPC2051: 100 V, 37 A

EPC2039: 80 V, 50 A

EPC2108: 60 V Dual with Sync Boot, 5.5 A / 0.5 A
EPC2107: 100 V Dual with Sync Boot, 3.8 A / 0.5 A
EPC2106: 100 V Half Bridge, 18 A
EPC2110: 120 V Dual Common Source, 20 A

EPC2012C: 200 V, 22 A

EPC2014C: 40 V , 60 A
EPC2007C: 100 V, 40 A

EPC2050: 350 V, 26 A

EPC8004: 40 V, 7.5 A
EPC8002: 65 V, 2 A
EPC8009: 65 V , 7.5 A
EPC8010: 100 V, 7.5 A

EPC2202: 80 V, 75 A – **AEC-Q101 Qualified**
EPC2212: 100 V, 75 A – **AEC-Q101 Qualified**
EPC2016C: 100 V, 75 A

EPC2049: 40 V, 175 A
EPC2045: 100 V, 130 A

EPC2019: 200 V, 42 A

EPC2046: 200 V, 55 A

EPC2112: 200 V, Integrated Driver GaN FET

EPC2115: 150 V, Dual Integrated Driver GaN FET

EPC2111: 30 V, Asymmetric Half Bridge, 140 A / 50 A

EPC2010C: 200 V, 90 A

EPC2015C: 40 V, 235 A
EPC2001C: 100 V, 150 A

EPC2047: 200 V, 160 A

EPC2030: 40 V, 495 A
EPC2031: 60 V, 450 A
EPC2029: 80 V, 360 A
EPC2032: 100 V, 340 A
EPC2033: 150 V, 260 A
EPC2034: 200 V, 140 A

EPC2023: 30 V, 590 A
EPC2024: 40 V, 550 A
EPC2020: 60 V, 470 A
EPC2021: 80 V, 420 A
EPC2206: 80 V, 390 A – **AEC-Q101 Qualified**
EPC2022: 100 V, 360 A

EPC2100: 30 V Asymmetrical Half Bridge, 400 A / 100 A
EPC2101: 60 V Asymmetrical Half Bridge, 350 A / 80 A
EPC2102: 60 V Symmetrical Half Bridge, 215 A
EPC2103: 80 V Asymmetrical Half Bridge, 195 A / 30 A
EPC2105: 80 V Asymmetrical Half Bridge, 320 A / 75 A
EPC2104: 100 V Symmetrical Half Bridge, 165 A

A Better Power Package:

- Double-sided cooling improves thermal performance
- Low inductance enables faster switching
- Elimination of plastic packages reduces size, cost, and improves reliability