EPC23101 – ePower™ Chipset

V_{IN} , 100 V

I_{Load} , 65 A

PRELIMINARY

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

EPC's ePower™ Stage and Chipset integrate input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with eGaN output FETs. Integration is implemented using EPC's proprietary GaN IC technology. The end result is a Power Stage that translates logic level input to high voltage and high current power output that is smaller in size, easier to manufacture, simpler to design and more efficient to operate.

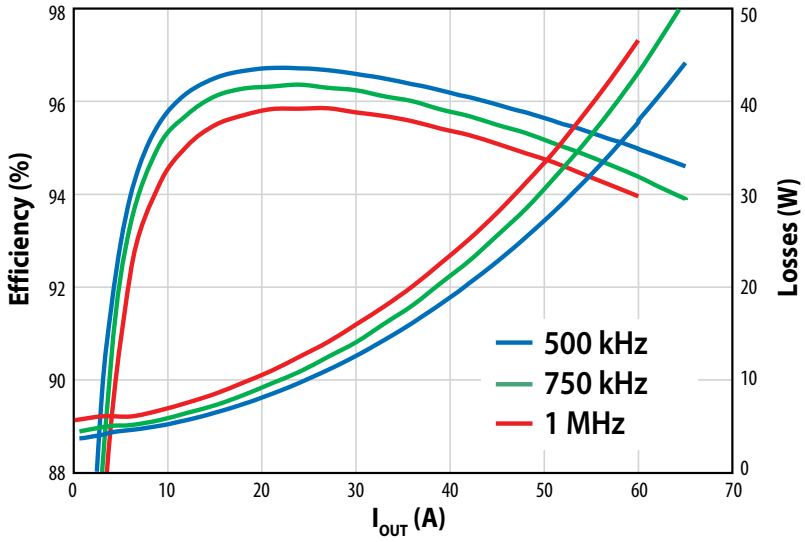
Key Parameters		
PARAMETER	**VALUE**	**UNIT**
Power Stage Load Current (1 MHz)	65 [1]	A
Operating PWM Frequency Range	3 [2]	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	
Nominal Bias Supply Voltage	5	

Output Current and PWM Frequency Ratings are functions of Operating Conditions. Appropriate derating should be applied to keep T_J at less than 125 °C. See Notes 1 & 2.

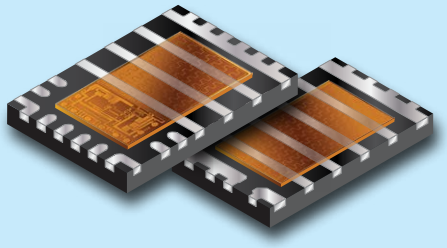
Chipset Information		
PART NUMBER	**Rated $R_{DS(on)}$ at 25°C**	**QFN Package Size (mm)**
EPC23101	3.3 mΩ	3.5 x 5
EPC2302	1.8 mΩ	3 x 5

All exposed pads feature wettable flanks that allow side wall solder inspection. High voltage and low voltage pads are separated by 0.6 mm spacing to meet IPC rules. Recommended to use EPC2302 as companion low side FET for the chipset.

Figure 1: Performance Curves



Buck Converter, V_{IN} = 48 V, V_{OUT} = 12 V, Deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, EPC23101 + EPC2302, Airflow = 1000 LFM. See See **EPC90142 Quick Start Guide** for details.



EPC23101 ePower™ Chipset

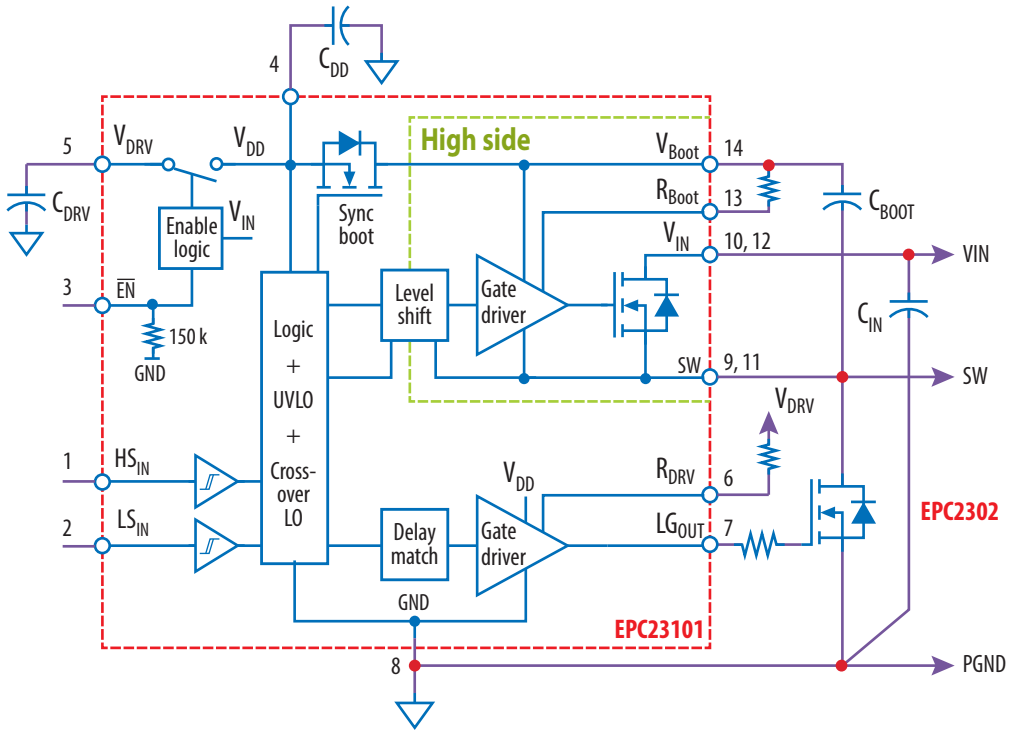
Applications

- Buck, Boost, Half-Bridge, Full Bridge or LLC Converters
- Motor Drive Inverter

Features

- Integrated high side eGaN® FET with internal gate driver and level shifter
- 5 V external bias supply
- 3.3 V or 5 V CMOS input logic levels
- Independent high side and low side control inputs
- Cross conduction lockout logic keeps both FETs off when logic inputs are both high at same time
- External resistors to tune SW switching times and over-voltage spikes above rail and below ground
- Robust level shifter operating for hard and soft switching conditions
- False trigger immunity from fast switching transients
- Synchronous charging for high side bootstrap supply
- Low quiescent current mode from external V_{DRV} supply when V_{DD} Disable Input pin is pulled up
- Undervoltage lockout for internal low side and high side bias supplies
- Active gate pull-down for HS FET and LS gate drive with loss of V_{DRV} supply
- Chipset of compatible high and low side devices in QFN packages with optimized pinouts between the two devices

Figure 2: Functional Block Diagram



General Description

The EPC23101 ePower™ IC integrates a half-bridge gate driver with an internal high side FET. It is designed as part of a chipset with a companion low side eGaN® FET such as the EPC2302. Integration is implemented using EPC's proprietary GaN IC technology. The high side monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with a high side eGaN output FET. The low side output FET is driven by the gate driver output of the GaN IC to configure a half-bridge power stage.

The on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Power loop inductance is minimized by compatible high side to low side pinout configuration that facilitates optimal layout technique. Switching times are tuned by external resistors to achieve 1–3 ns rise and fall times from 0–48 V at full load current. Over-voltage spikes can be controlled to less than +10 V above rail and –10 V below ground during hard switching transitions by choosing the tuning resistors, R_{BOOT} and R_{DRV}.

The EPC23101 IC only requires an external 5 V V_{DRV} power supply. Internal low side and high side power supplies, V_{DD} and V_{BOOT}, are generated from the external supply via a series connected switch. The internal supplies can be cut off to save quiescent power by turning off the switch with 5 V applied to the $\overline{EN}$ pin.

The charging path for the floating bootstrap supply is activated with L_{SIN} logic. It uses eGaN FET as the series switch that minimizes power losses by eliminating reverse recovery. This synchronous bootstrap charging circuit also minimizes voltage drop in the charging path.

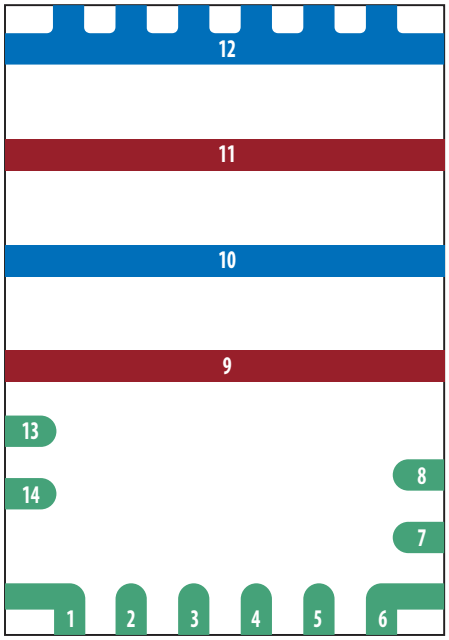
Robust level shifters from low side to high side channels are designed to operate correctly even at large negative clamped voltage and to avoid false trigger from fast dv/dt transients including those driven by external sources or other phases.

Protection is provided by high side and low side under-voltage lockout to keep both FETs off at low supply voltages. If the supply voltages drop even lower or are lost while V_{IN} is active at greater than 10 V, another active pull-down circuit is used with biasing from V_{IN} to prevent destructive turn-on of both FETs from gate to drain leakage..

The EPC23101 IC is capable of interfacing to digital controllers that use standard 3.3 V or 5 V CMOS logic levels. Separate and independent high side and low side logic control inputs allow external controllers to set fixed or adaptive dead times for optimal operating efficiency. Cross conduction prevention logic keeps both FETs off when logic inputs are both high at the same time.

The FET gate drive voltages are derived from the internal low side and high side power supplies. Full gate drive voltages are only available after the HS_{IN} and LS_{IN} PWM inputs start to operate for a few cycles.

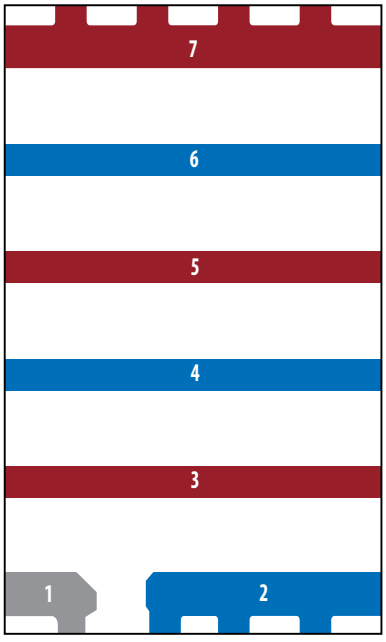
Figure 3: EPC23101 Transparent Top View



Pin	Pin Name	Pin Type	Description
1	HS_{IN}	I	High side PWM logic input, level referenced to GND. Internal pull-down resistor is connected between HS_{IN} and GND.
2	LS_{IN}	I	Low side PWM logic input, level referenced to GND. Internal pull-down resistor is connected between LS_{IN} and GND.
3	$\overline{EN}$	I	V_{DD} disable input, level referenced to GND. Internal VDD will be disabled when $\overline{EN}$ is connected to V_{DRV}. V_{DD} will follow V_{DRV} when $\overline{EN}$ is connected to GND. Internal pull-down resistor is connected between $\overline{EN}$ and GND.
4	V_{DD}	S	Internal power supply referenced to GND, connect a bypass capacitor from V_{DD} to GND.
5	V_{DRV}	S	External 5 V nominal power supply referenced to GND, connect a bypass capacitor from V_{DRV} to GND.
6	R_{DRV}	O	Insert resistor between R_{DRV} to V_{DRV} to control the turn-on slew rate of the driven low side FET.
7	LG_{OUT}	O	Low side gate drive output to driven low side FET. Maintain short loop between LG_{OUT} and kelvin source connection of low side FET to minimize common mode inductance.
8	GND	S, O	Logic ground. Connect bypass capacitors between operating bias supplies, V_{DRV} and V_{DD} to GND. Low side output gate driver is also referenced to same GND pin.
9, 11	SW	P, S	Output switching node. Connected to output of half-bridge power stage. The floating bootstrap power supply, V_{BOOT}, is also referenced to SW.
10, 12	V_{IN}	P	Power bus input. Connected to drain terminal of internal high side FET. Connect power loop capacitors from V_{IN} to PGND or power source terminals of low side FET.
13	R_{BOOT}	O	Insert resistor between R_{BOOT} to V_{BOOT} to control the turn-on slew rate of the internal high side FET.
14	V_{BOOT}	S	Floating bootstrap power supply referenced to SW, connect an external bypass capacitor from V_{BOOT} to SW.

Pin Type: P = Power, S = Bias Supplies, I = Logic Inputs, O = Gate Drive Output

Figure 4: EPC2302 Transparent Top View



Pin	Description
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
V_{IN}	Input Voltage (V_{IN} to GND)		100	V
$V_{SW(continuous)}$	Output Switching Node (SW to GND), Continuous		100	
V_{DRV}	External Bias Supply (V_{DRV} to GND)		6	
V_{DD}	Internal Low Side Supply Voltage (V_{DD} to GND)		6	
$V_{BOOT} - V_{SW}$	Internal High Side Supply Voltage (V_{BOOT} to SW)		6	
LG_{OUT}	Low Side Gate Drive Output (LG_{OUT} to GND)		6	
HS_{IN}, LS_{IN}	PWM Logic Inputs		5.5	
$\overline{EN}$	V_{DD} Disable Input		5.5	
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-55	150	

ESD Ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)	+/-1000		V
CDM	Charged-device model (JEDEC JESD22-C101)	+/-500		

Thermal Characteristics

$R_{\theta JA\_JEDEC}$ is measured using JESD51-2 standard setup with 1 cubic foot enclosure with no forced air cooling, heat dissipated only through natural convection. The test used JEDEC Standard 4-layers PCB with 2oz top and bottom surface layers and 1oz buried layers. $R_{\theta JA\_EVB}$ is measured using EPC90142 EVB with no forced air cooling, this rating is more indicative of actual application environment.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{\theta JC\_Top}$	Thermal Resistance, Junction-to-Case (Top surface of exposed die substrate)	0.4	°C/W
$R_{\theta JB\_Bottom}$	Thermal Resistance, Junction-to-Board (At solder joints of V_{IN} and SW PCB pads)	3	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	43	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90142 EVB)	25	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Recommended Operating Conditions					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage (V_{IN} to GND)	10 [3]		80	V
$V_{SW(Q3\ Mode)}$	Output Switch Node, 3rd Quadrant Mode [4]	-2.5		V_{IN} + 2.5	
$V_{SW(pulse2ns)}$	Output Switch Node, Transient PW<2 ns [5]	-10		V_{IN} +10	
V_{DRV}	External Bias Supply (V_{DRV} to GND)	4.75	5	5.5	
V_{DD}	Internal Low Side Supply Voltage (V_{DD} to GND)	4.75	5	5.5	
$V_{BOOT} - V_{SW}$	Internal High Side Supply Voltage (V_{BOOT} to SW)	4.75	5	5.5	
LG_{OUT}	Low Side Gate Drive Output (LG_{OUT} to GND)	4.75	5	5.5	
HS_{IN}, LS_{IN}	PWM Logic Inputs [6]	0		5	
$\overline{EN}$	V_{DD} Disable Input [3]	0		5	
T_J	Operating Junction Temperature	-40		125	°C
PW_min	Minimum input On or Off Pulse Duration, 50% to 50% width	20			ns
PW_max	Maximum input On or Off Pulse Duration, 50% to 50% width			200	µs

Electrical Characteristics

Nominal V_{IN} = 48 V, V_{DRV} = V_{DD} = 5 V and (V_{BOOT} – VSW) = 5 V. CL = 4000 pF. All typical ratings are specified at T_A = 25˚C unless otherwise indicated. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Side Power Supply						
$IDRV_Q$	Off State Total Quiescent Current	$HS_{IN}/LS_{IN}/EN$ = 0 V, V_{DRV} = V_{DD} = 5 V		10		mA
$IDRV_{100kHz}$	Total Operating Current @100 kHz	PWM = 100 kHz, 50% On-Time		18		
$IDRV_{1MHz}$	Total Operating Current @1 MHz	PWM = 1 MHz, 50% On-Time		37		
$IIN_{disable}$	V_{IN} Quiescent Current at Disable Mode	$\overline{EN}$ = V_{DRV} = 5 V, V_{IN} = 48 V			600	µA
$IDRV_{disable}$	V_{DRV} Quiescent Current at Disable Mode	$\overline{EN}$ = V_{DRV} = 5 V, V_{IN} = 48 V			50	
Bootstrap Power Supply						
$IBOOT_Q$	Off State Bootstrap Supply Current	HS_{IN} = 0 V, (V_{BOOT} – V_{SW}) = 5 V		6		mA
$IBOOT_{100kHz}$	Bootstrap Supply Current @100 kHz	HS PWM = 100 kHz, 50% On-Time		8		
$IBOOT_{1MHz}$	Bootstrap Supply Current @1 MHz	HS PWM = 1 MHz, 50% On-Time		20		
V_{SYNC_BOOT}	Sync Boot Generated (V_{BOOT} -V_{SW})	ISYNC_BOOT = 20 mA		4.75		V
Undervoltage Lockout						
VDD_{UVLO+}	UVLO Trip Level V_{DD} Rising	LS_{IN} = 5 V, V_{DD} Ramps Up		4.0		V
VDD_{HYST}	UVLO V_{DD} Falling Hysteresis	LS_{IN} = 5 V, V_{DD} Ramps Down		0.5		
$VBOOT_{UVLO+}$	UVLO Trip Level (V_{BOOT} - VSW) Rising	HS_{IN} = 5 V, V_{BOOT} Ramps Up		4.0		
$VBOOT_{HYST}$	UVLO (V_{BOOT} - VSW) Falling Hysteresis	HS_{IN} = 5 V, V_{BOOT} Ramps Down		0.5		
Logic Input Pins						
V_{IH}	High-level Logic Threshold	HS_{IN}, LSIN Rising	2.4			V
V_{IL}	Low-level Logic Threshold	HS_{IN}, LSIN Falling			0.8	
V_{IHYST}	Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		0.3		
R_{IN}	HS_{IN} and LS_{IN} Pull-Down Resistance	HS_{IN}, LS_{IN} = 5 V		6.5		kΩ
V_{DD} Disable Input						
V_{TH_EN}	$\overline{EN}$ Input Threshold	V_{DRV} = 5 V	3.3			V
R_{EN}	$\overline{EN}$ Pull-Down Resistance	$\overline{EN}$ = 5 V		150		kΩ
Low Side Gate Drive Output						
$R_{DS(on)\_PU}$	Gate Output Pull-Up FET $R_{DS(on)}$	R_{DRV} = V_{DRV}		0.4		Ω
$R_{DS(on)\_PD}$	Gate Output Pull-Down FET $R_{DS(on)}$			0.4		
I_{PU}	Short Circuit Pull-Up Current	R_{DRV} = V_{DRV}, LG_{OUT} = 0 V		5		A
I_{PD}	Short Circuit Pull-Down Current	LG_{OUT} = V_{DRV}		5		
High Side Internal Power FET						
$R_{DS(on)\_HS}$	High Side FET $R_{DS(on)}$	I_{DS} = +/-10 A, HS_{IN} = 5 V, LS_{IN} = 0 V		2.6	3.3	mΩ
$V_{HS\_DS\_Clamp}$	High Side 3rd Quadrant Clamp	I_{DS} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-1.5		V
I_{LEAK_VIN-SW}	Leakage Current (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 100 V, SW = 0 V			100	µA
C_{SW}	Output Capacitance (SW to GND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		82		pF
C_{OSS_HSFET}	Output Capacitance (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		630		
Q_{OSS_HSFET}	Output Charge (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		50		nC
E_{QOSS}	Output Capacitance Stored Energy	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		0.9		µJ
$E_{ON\_HS\_0}$	Turn-On Switching Energy (HS_FET)	HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10 A		5		
$E_{ON\_HS\_1}$		HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10 A		9		
E_{OFF_HS}	Turn-Off Switching Energy (HS_FET)	HS Turn-Off, SW = 48 V to 0 V, I_{LOAD} = 10 A		0.3		

Electrical Characteristics *(continued)*

Electrical Characteristics (continued)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Characteristics (Logic Input to Output Switching Node) See Figure 6. Timing Diagram and Test Circuit EPC23101 + EPC2302)						
$t\_delay_{HS\_on}$	High-Side On Propagation Delay	SW = 0 V and HS FET Turn-On		20		ns
$t\_delay_{LS\_on}$	Low-Side On Propagation Delay	SW = 48 V and LS FET Turn-On		20		
$t\_delay_{HS\_off}$	High-Side Off Propagation Delay	SW = 48 V and HS FET Turn-Off		20		
$t\_delay_{LS\_off}$	Low-Side Off Propagation Delay	SW = 0 V and LS FET Turn-Off		20		
t_match_{on}	Delay Matching LS_{off} to HS_{on}	LS Turn-Off to HS Turn-On		0		
t_match_{off}	Delay Matching HS_{off} to LS_{on}	HS Turn-Off to LS Turn-On		0		
$t\_rise_{SW\_HS0}$	SW Rise Time at High Side FET Turn-On (Buck Mode, Hard Switching)	HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 0 Ω, I_{Load} = 5 A		1.5		
$t\_rise_{SW\_HS1}$		HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{Load} = 5 A		3		
$t\_fall_{SW\_LS0}$	SW Fall Time at Low Side FET Turn-On (Boost Mode, Hard Switching)	LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV} = 0 Ω, I_{Load} = 5 A		1.5		
$t\_fall_{SW\_LS1}$		LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV}= 2.2 Ω , I_{Load} = 5 A		3		
$t\_rise_{LGOUT\_0}$	Low Side Gate Drive Rise Time	LG_{OUT} Turn-On, R_{DRV} = 0 Ω, CL = 4000 pF		4.5		
$t\_rise_{LGOUT\_1}$		LG_{OUT} Turn-On, R_{DRV} = 2.2 Ω, CL = 4000 pF		9		
$t\_fallL_{GOUT\_0}$	Low Side Gate Drive Fall Time	LG_{OUT} Turn-Off, R_{GATE} = 0 Ω, CL = 4000 pF		3		

Dynamic Characteristics Parameter Definition

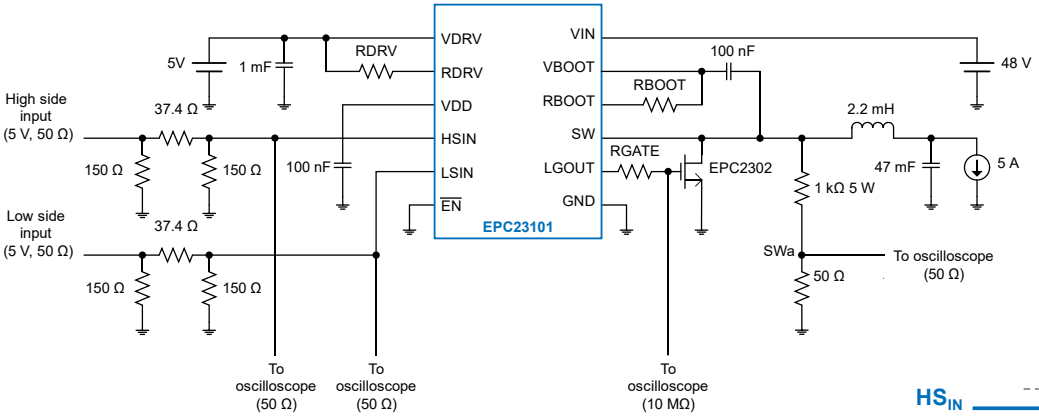


Figure 5a: Test Circuit for Dynamic Characteristics

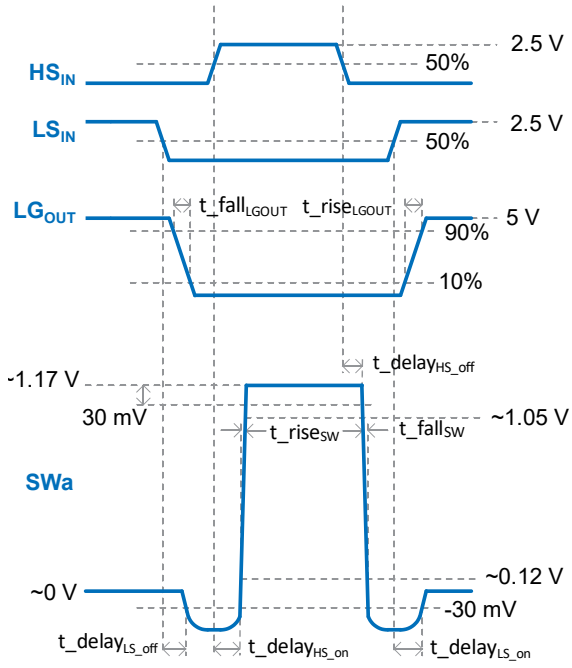


Figure 5b: Logic Input to Output Switching Node Timing Diagram

Truth Table					
V_{DD}	V_{BOOT} – V_{SW}	HS_{IN}	LS_{IN}	HS FET	LS FET
<UVLO	–	–	–	OFF	OFF
>UVLO	<UVLO	–	0	OFF	OFF
>UVLO	<UVLO	–	1	OFF	ON [7]
>UVLO		0	0	OFF	OFF
		0	1	OFF	ON
		1	0	ON	OFF
		1	1	OFF [8]	

NOTES:

Note 1: Power Stage load current rating is measured using a buck converter application circuit with V_{IN} = 48 V, V_{OUT} = 13.8 V, PWM frequency = 500 kHz, PCB mounted using EPC90142 Evaluation Board, EPC23101 as high side FET and EPC2302 as low side FET, top side heat sink for both devices, 800 LFM airflow, operating at ambient temperature of 25°C with T_J not to exceed 125°C. The rated Power Stage load current specification depends on the application circuit topology, driven low side FET characteristics, duty cycle, power dissipation, maximum allowed junction temperature and thermal management techniques and mechanical stress limit imposed by electromigration.

Note 2: Operating PWM switching frequency range is a function of the characteristics of the driven low side FET, power dissipation, maximum allowed junction temperature and minimum duty cycle. The EPC23101 device is capable of operating above 3 MHz PWM switching frequency given appropriate cooling but users need to derate the maximum output current depending on thermal management technique not to exceed T_J = 125°C.

Note 3: The minimum input voltage (V_{IN}) should be >= 10 V for the IC to be enabled. Below the minimum V_{IN} the pass-transistor between V_{DRV} and V_{DD} will be off. Same condition when V_{DD} disable pin, $\overline{EN}$, is connected to 5 V.

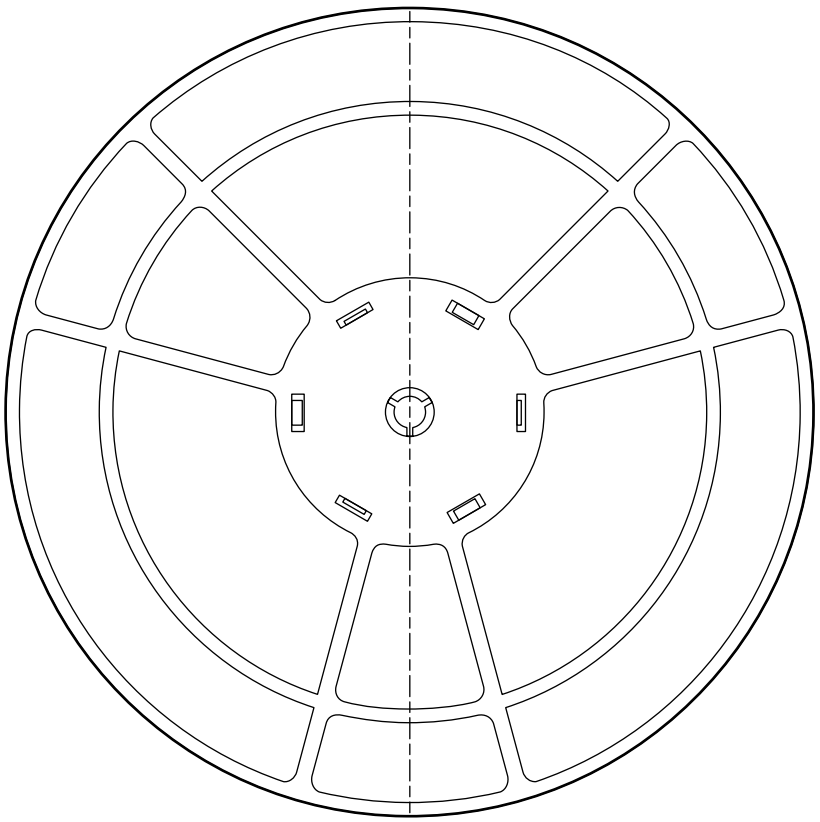
Note 4: The output switching node (SW) is clamped above V_{IN} by the HS FET or below GND by the LS FET at their respective source drain voltage in the 3rd quadrant. This is an operating condition when both HS and LS FETs are in the off states during the dead time period which is set by the application circuit with typical value of 15 ns. The Absolute Minimum Rating is determined by LS FET 3rd quadrant clamp voltage below GND. Conversely the Absolute Maximum Rating is determined by HS FET 3rd quadrant clamp voltage above V_{IN}. The time duration that the device can stay in the negative clamp voltage region is subjected to the amount of load current, power dissipation and maximum allowed junction temperature.

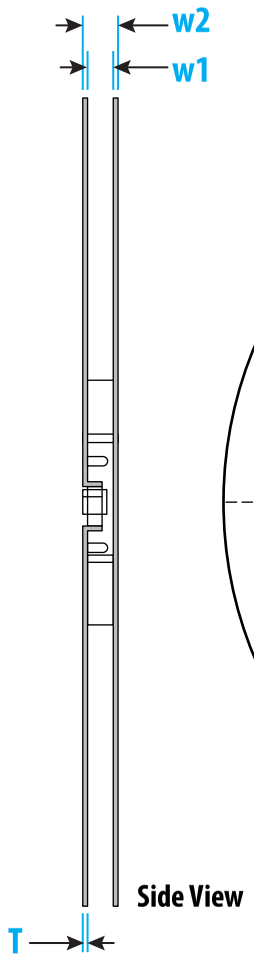
Note 5: During HS FET or LS FET turn-on transitions with hard switching conditions, the fast di/dt of the HS FET or LS FET coupled with the power loop inductance ($V_{Peak} = L_{Power\ loop} \cdot di/dt$) would cause a transient over-voltage spike above V_{IN} or below GND. The Absolute Minimum Rating is amount of peak voltage spike, caused by LS FET di/dt, below GND for less than 2 ns pulse duration. Conversely the Absolute Maximum Rating is amount of peak voltage spike, caused by HS FET di/dt, above VIN, for less than 2 ns pulse duration.

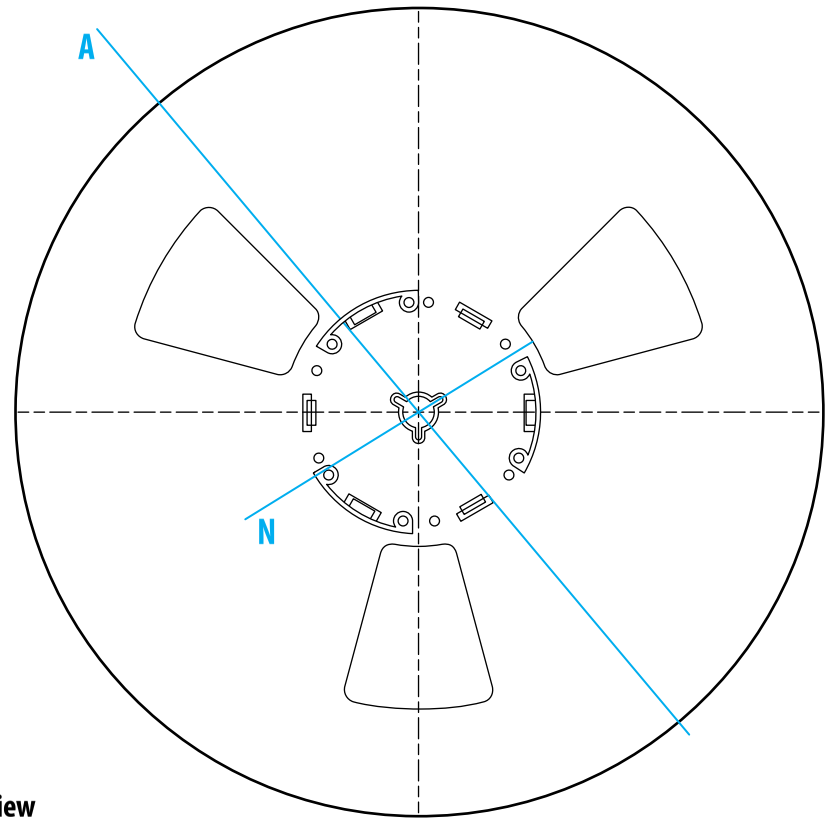
Note 6: For interfacing with analog controller operating from 12 V_{CC} and outputting a 12 V drive signal, a resistor network in series should be inserted to divide the voltage to acceptable V_{IH} level and limit the input current into the logic input pins H_{IN} and L_{IN} which is clamped to the V_{DD} supply by ESD protection network.

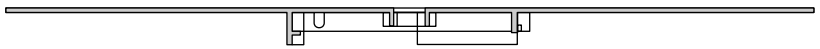
Note 7: L_{IN} commands LS FET to turn-on to charge bootstrap supply through sync boot.

Note 8: Internal logic follows HS_{IN}, LS_{IN} respectively but cross conduction lockout logic prevents both HS and LS FETs to turn on together as commanded if both HS_{IN} and LS_{IN} are set to logic "high".

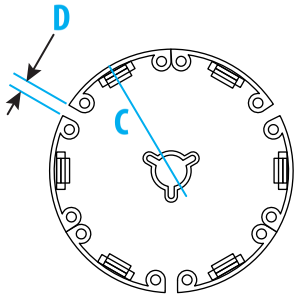




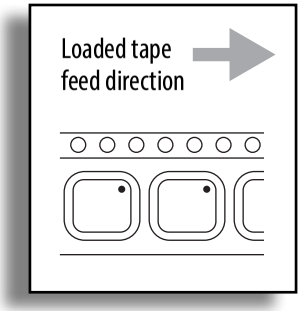




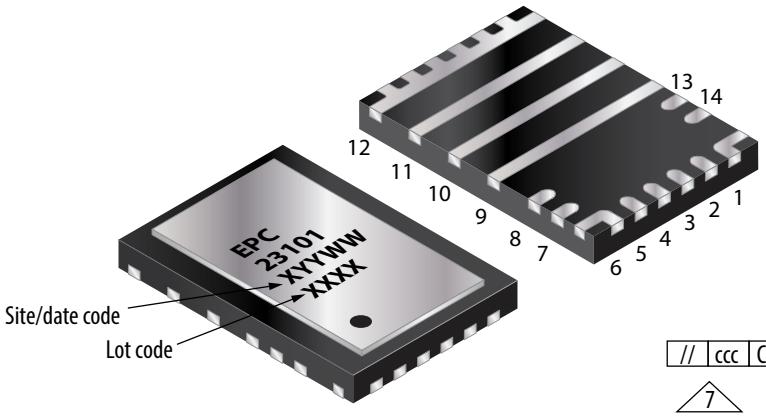
Top View Detail



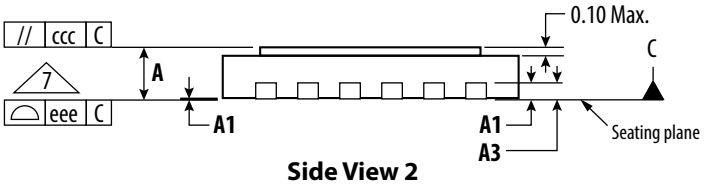
Bottom View Detail



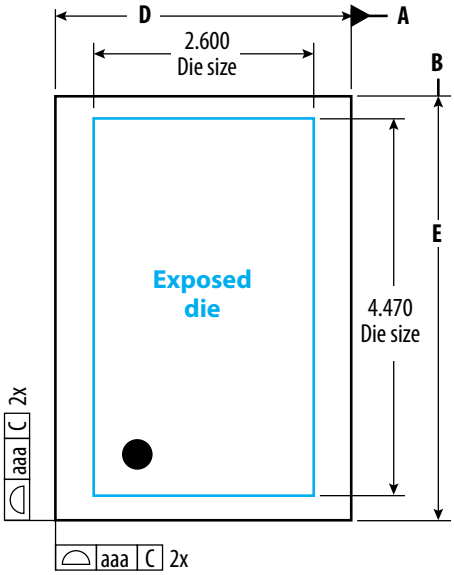
Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5



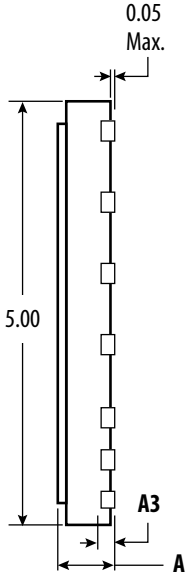
Pads 1-8,13 and 14 are IC pins;
Pads 9 and 11 are SW pins ;
Pads 10 and 12 are V_{IN} pins



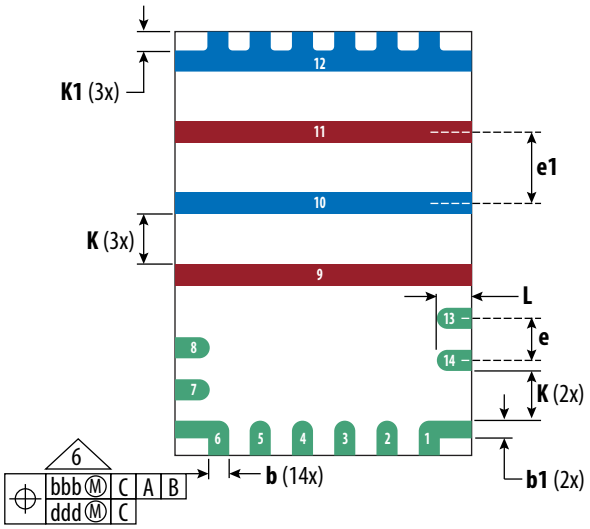
Side View 2



Top View



Side View 1



Bottom View

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	6
b1	0.15	0.20	0.25	6
D		3.50 BSC		
E		5.00 BSC		
e		0.50 BSC		
e1		0.85 BSC		
K	0.55	0.60	0.65	
K1	0.15	0.20	0.25	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		14		3
ND		6		5
NE		7		5
Notes		1, 2		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. **ND** and **NE** refer to the number of terminals on each **D** and **E** side respectively.
6. Dimension **b** applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
7. Coplanarity applies to the terminals and all the other bottom surface metallization.

Errata Sheet

STATUS	VERSION	DATE	REMARK
ENGRT	1.1	12/09/2022	The following features and parameters do not meet the datasheet description and specifications: 1) The maximum operating VIN voltage should not exceed 64 V 2) The maximum transient voltage at the output switch node SW, should not exceed 70 V. Recommend to use at least 4.7 Ω for R_{BOOT} and R_{DRV} to module the over-voltage spike above VIN rail and below PGND to less than 10 V.