EPC23102 – ePower™ Stage IC

V_{IN}, 100 V

I_{LOAD}, 35 A

PRELIMINARY

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

The ePower™ Stage IC Product Family integrates input logic interface, high-side level shifting, synchronous bootstrap charging and gate drivers along with eGaN output FETs into one monolithic integrated-circuit using EPC's proprietary GaN IC technology. The result is a Power Stage IC that translates logic level control signals into a high voltage and high current power stage that is simpler to design, smaller in size and easier to manufacture while being more efficient to operate.

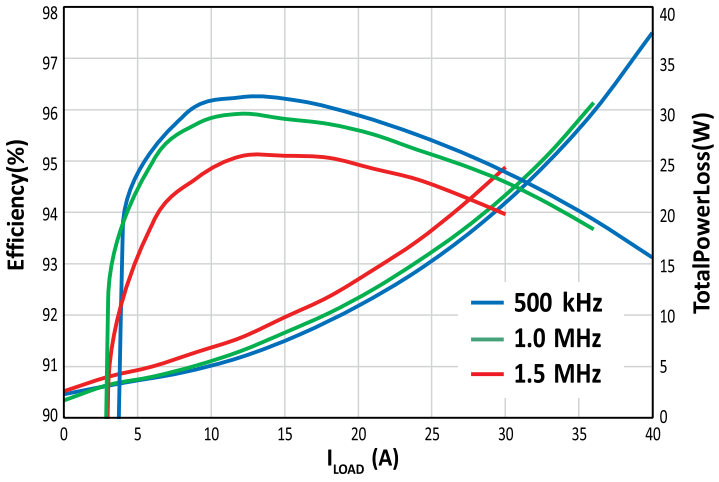
Key parameters		
PARAMETER	**VALUE**	**UNIT**
Power Stage Load Current (1 MHz)	35	A
Pulsed current (25°C, T_{pulse} = 300 µs)	140	
Operating PWM Frequency (Minimum)	5	kHz
Operating PWM Frequency (Maximum)	3	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	
Nominal Bias Supply Voltage	5	

Output Current and PWM Frequency Ratings are specified at ambient temperature of 25°C. See Application Information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

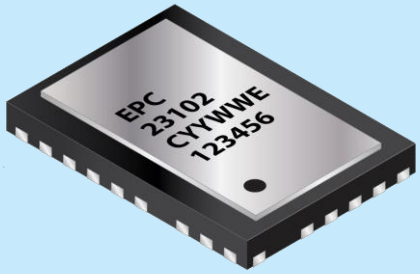
Device information		
PART NUMBER	**Rated $R_{DS(on)}$ for HS and LS FETs at 25 °C**	**QFN Package Size (mm)**
EPC23102	6.6 mΩ + 6.6 mΩ	3.5 x 5

All exposed pads feature wettable flanks that allow side wall solder inspection. High voltage and low voltage pads are separated by 0.6mm spacing to meet IPC rules.

Figure 1: Performance curves



Buck converter, V_{IN} = 48 V, V_{OUT} = 12 V, deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, top side heatsink attached, airflow = 500 LFM, T_A = 25°C, using **EPC90147 evaluation board**.



EPC23102 ePower™ Stage IC

Package size: 3.5 x 5 mm

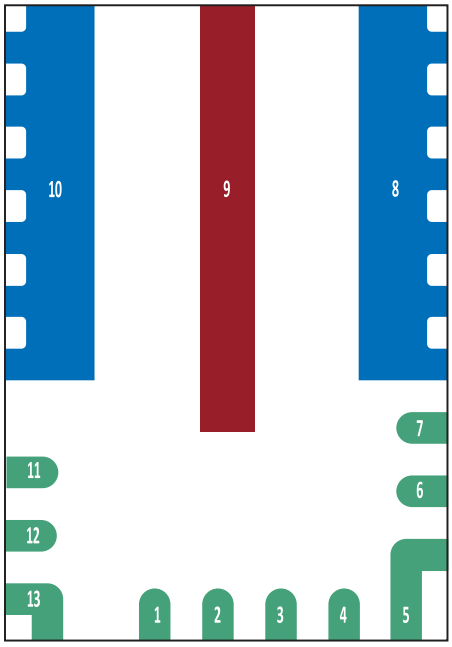
Applications

- Buck, boost, buck-boost converters
- Half-bridge, full bridge LLC converters
- Motor drive inverter
- Class D audio amplifier

Features

- Integrated high-side and low-side eGaN® FET with internal gate driver and level shifter
- 5 V external bias supply
- 3.3 V or 5 V CMOS input logic levels
- Independent high side and low side control inputs
- Logic lockout commands both FETs off when inputs are both high at same time
- External resistors to tune SW switching times
- Robust level shifter operation for hard and soft switching conditions
- False trigger immunity from fast switching transients
- Synchronous charging for high-side bootstrap supply
- Low quiescent current mode
- Power-on-reset for low side andand high side power supplies
- Active gate pull-down for HS and LS FET allowing for flexible power up sequencing
- Thermally enhanced QFN package with exposed top for low thermal resistance from junction to top-side heatsink

Figure 2: EPC23102 Quad Flat No-Lead (QFN) package (transparent top view)



Transparent Top View

EPC23102 pinout description

Pin	Pin Name	Pin Type	Description
1	HSIN	L	High-side PWM logic input referenced to AGND. Internal pull-down resistor is connected between HSIN and AGND.
2	LSIN	L	Low-side PWM logic input referenced to AGND. Internal pull-down resistor is connected between LSIN and AGND.
3	SD	L	VDD disable input referenced to AGND. Internal VDD will be disabled when SD is pulled up to VDRV or external 5 V source. Internal pull-down resistor is connected between SD and AGND, thereby VDD will follow VDRV with SD connected to AGND by default.
4	VDD	S	Internal power supply referenced to AGND, connect a bypass capacitor from VDD to AGND.
5	VDRV	S	External 5 V nominal power supply referenced to AGND, connect a bypass capacitor from VDRV to AGND.
6	RDRV	G	Insert resistor between RDRV to VDRV to control the turn-on slew rate of the driven low side FET.
7	AGND	S	Logic ground. Connect bypass capacitors between operating bias supplies, VDRV and VDD, to AGND. Internal IC connection between AGND and PGND. Use star ground external connection with PGND to system ground.
8	PGND	P	Input power supply ground return. Connected to source terminal of internal low-side FET. Connect power loop capacitors from VIN to PGND.
9	SW	P	Output switching node. Connected to output of half-bridge power stage. SW pin connects the source terminal of high-side FET to the drain terminal of the low-side FET.
10	VIN	P	Power bus input. Connected to drain terminal of internal high side FET. Connect power loop capacitors from VIN to PGND or power source terminals of low-side FET.
11	VPHASE	S	VPHASE is Kelvin connected to SW, the output switching node. Connect an external bootstrap capacitor, Cboot, between VBOOT and VPHASE.
12	RBOOT	G	Insert resistor between RBOOT and VBOOT to control the turn-on slew rate of the internal high-side FET.
13	VBOOT	S	Floating bootstrap power supply referenced to VPHASE (=SW). Connect an external bootstrap capacitor, Cboot, between VBOOT and VPHASE.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs, G = Gate Drive Adjust

Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to PGND (=AGND) unless indicated otherwise.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
VIN	Input voltage (VIN to PGND)		100	V
$SW_{(continuous)}$	Output switching node (SW to PGND), continuous		100	
VDRV	External bias supply (VDRV to AGND)		6	
VDD	Internal low side supply voltage (VDD to AGND)		6	
VBOOT – VPHASE	Internal high side supply voltage (VBOOT to VPHASE), VPHASE = SW		6	
HSIN, LSIN	PWM logic inputs (HSIN to AGND and LSIN to AGND)	-1	5.5	
SD	VDD disable input (SD to AGND)	-1	5.5	
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	

ESD ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)	+/-1000		V
CDM	Charged-device model (JEDEC JESD22-C101)	+/-500		

Thermal characteristics

$R_{\theta JA\_JEDEC}$ is measured using JESD51-2 standard setup with 1 cubic foot enclosure with no forced air cooling, heat dissipated only through natural convection. The test used JEDEC Standard 4-layers PCB with 2 oz top and bottom surface layers and 1 oz buried layers. $R_{\theta JA\_EVB}$ is measured using EPC90147 EVB with no forced air cooling, this rating is more indicative of actual application environment.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{\theta JC\_Top}$	Thermal resistance, junction-to-case (Top surface of exposed die substrate)	0.4	°C/W
$R_{\theta JB\_Bottom}$	Thermal resistance, junction-to-board (At solder joints of VIN, SW and PGND pads)	3	
$R_{\theta JA\_JEDEC}$	Thermal resistance, junction-to-ambient (using JEDEC 51-2 PCB)	43	
$R_{\theta JA\_EVB}$	Thermal resistance, junction-to-ambient (using EPC90147 EVB)	25	

Recommended operating conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to PGND (= AGND) unless indicated otherwise.

Recommended Operating Condition					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
VIN	Input voltage (VIN to PGND) , with shutdown function (default)	10		80	V
VIN_no_SD	Input voltage (VIN to PGND), without shutdown function (note 1)	0			
$SW_{(Q3\ Mode)}$	Output switch node, 3rd quadrant mode	-2.5		V_{IN} + 2.5	
$SW_{(pulse2ns)}$	Output switch node, transient PW < 2 ns	-10		V_{IN} +10	
VDRV	External bias supply (VDRV to AGND)	4.75	5	5.5	
VDD	Internal low side supply voltage (VDD to AGND)	4.75	5	5.5	
VBOOT – VPHASE	Internal high side supply voltage ($VBOOT_T$ to VPHASE), VPHASE = SW	4.75	5	5.5	
HSIN, LSIN	PWM logic inputs	0		5	
SD	VDD shutdown input	0		5	
$T_{J,op}$	Operating junction temperature	-40		125	°C

Note 1: tie VDD and VDRV together to bypass shutdown function, see figure 9.

Electrical Characteristics

Nominal VIN = 48 V, VDRV = VDD = 5 V and (VBOOT – VPHASE) = 5 V. All typical ratings are specified at T_A = 25°C unless otherwise indicated. All voltage parameters are absolute voltages referenced to PGND (= AGND) unless indicated otherwise. (1)

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply						
I_{DRV_Q}	Off State Total Quiescent Current	HSIN/LSIN/SD = 0 V, VDRV = VDD = 5 V, SW floating		10	*TBD*	mA
I_{DRV_100kHz}	Total Operating Current @100 kHz	PWM = 100 kHz, 50% On-Time, includes bootstrap current		16	*TBD*	
I_{DRV_1MHz}	Total Operating Current @1 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		32	*TBD*	
$I_{VIN\_disable}$	VIN Quiescent Current at Disable Mode	SD = VDRV = 5 V, VIN = 48 V		110	600	µA
$I_{DRV\_disable}$	VDRV Quiescent Current at Disable Mode	SD = VDRV = 5 V, VIN = 48 V		1	50	
Bootstrap Power Supply						
I_{BOOT_Q}	Off State Bootstrap Supply Current	HSIN/LSIN/SD = 0 V, (VBOOT – VPHASE) = 5 V		6	*TBD*	mA
I_{BOOT_100kHz}	Bootstrap Supply Current @100 kHz	HS PWM = 100 kHz, 50% On-Time		7	*TBD*	
I_{BOOT_1MHz}	Bootstrap Supply Current @1 MHz	HS PWM = 1 MHz, 50% On-Time		15	*TBD*	
$Ron_{\_SYNC\_BOOT}$	On resistance of Synch-boot FET	I_{SYNC_BOOT} = 20 mA		2.5		Ω
Power On Reset						
V_{DD_POR+}	POR Trip Level V_{DD} Rising	LSIN = 5 V, VDD Ramps Up	*TBD*	3.5	*TBD*	V
$V_{DD\_POR\_HYST}$	POR V_{DD} Falling Hysteresis	LSIN = 5 V, VDD Ramps Down		0.09		
V_{BOOT_POR+}	POR Trip Level (VBOOT - VPHASE) Rising	HSIN = 5 V, VBOOT Ramps Up	*TBD*	3.4	*TBD*	
$V_{BOOT\_POR\_HYST}$	POR (VBOOT - VPHASE) Falling Hysteresis	HSIN = 5 V, VBOOT Ramps Down		0.07		
Logic Input Pins						
PW_min	Minimum Input On or Off Pulse Duration	50% to 50% width , LIN and HIN	30			ns
PW_max	Maximum Input On or Off Pulse Duration	50% to 50% width , LIN and HIN			200	µs
V_{IH}	High-level Logic Threshold	HSIN, LSIN Rising	2.4			V
V_{IL}	Low-level Logic Threshold	HSIN, LSIN Falling			0.8	
V_{IHYST}	Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		0.4		
R_{IN}	HSIN and LSIN Pull-Down Resistance	HSIN, LSIN = 5 V		5.0	*TBD*	kΩ
V_{DD} Shutdown						
V_{TH_EN}	SD Input Threshold	VDRV = 5 V	3.3			V
R_{EN}	SD Pull-Down Resistance	SD = 5 V	*TBD*	200		kΩ

Electrical characteristics *(continued)*

Electrical Characteristics (continued)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
High Side Internal Power FET						
$R_{DS(on)\_HS}$	High Side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, HSIN = 5 V, LSIN = 0 V		5.2	6.6	mΩ
$V_{HS\_DS\_Clamp}$	High Side 3rd Quadrant Clamp	I_{LOAD} = - 10 A, HSIN & LSIN = 0 V		-2		V
I_{LEAK_VIN-SW}	Leakage Current (VIN to SW)	HSIN = 0 V, V_{IN} = 100 V, SW = 0 V			100	µA
C_{WELL}	HV-Well Capacitance (SW to PGND)	HSIN = 0 V, V_{IN} = 48 V, SW = 48 V		61		pF
C_{OSS_HSFET}	Output Capacitance (VIN to SW)	HSIN = 0 V, V_{IN} = 48 V, SW = 0 V		342		
Q_{OSS_HSFET}	Output Charge (VIN to SW)	HSIN = 0 V, V_{IN} = 48 V, SW = 0 V		28		nC
E_{QOSS_HSFET}	Output Capacitance Stored Energy	HSIN = 0 V, V_{IN} = 48 V, SW = 0 V		0.5		µJ
$E_{ON\_HS\_0}$	Turn-On Switching Energy (HS_FET)	HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10 A		2.5		
$E_{ON\_HS\_1}$		HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10 A		4.5		
E_{OFF_HS}	Turn-Off Switching Energy (HS_FET)	HS Turn-Off, SW = 48 V to 0 V, I_{LOAD} = 10 A		0.15		
Low Side Internal Power FET						
$R_{DS(on)\_HS}$	Low Side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, LSIN = 5 V, HSIN = 0 V		5.2	6.6	mΩ
$V_{LS\_DS\_Clamp}$	Low Side 3rd Quadrant Clamp	I_{LOAD} = - 10 A, HSIN & LSIN = 0 V		-2		V
$I_{LEAK\_SW-PGND}$	Leakage Current (SW to PGND)	LSIN = 0 V, V_{IN} = 100 V, SW = 100 V			100	µA
C_{OSS_LSFET}	Output Capacitance (SW to PGND)	LSIN = 0 V, SW = 48 V		343		pF
Q_{OSS_LSFET}	Output Charge (SW to PGND)	LSIN = 0 V, SW = 48 V		29		nC
E_{QOSS_LSFET}	Output Capacitance Stored Energy	LSIN = 0 V, SW = 48 V,		0.53		µJ
$E_{ON\_LS\_0}$	Turn-On Switching Energy (LS_FET)	LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10A		2.5		
$E_{ON\_LS\_1}$		LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10A		4.5		
E_{OFF_LS}	Turn-Off Switching Energy (LS_FET)	LS Turn-Off, SW = 0 V to 48 V, I_{LOAD} = 10 A		0.15		
Dynamic Characteristics (Logic Input to Output Switching Node) See Figure 3a and 3b for Timing Diagram and Test Circuit)						
$t\_delay_{HS\_on}$	High-Side On Propagation Delay	SW = 0 V and HS FET Turn-On		36		ns
$t\_delay_{LS\_on}$	Low-Side On Propagation Delay	SW = 48 V and LS FET Turn-On		36		
$t\_delay_{HS\_off}$	High-Side Off Propagation Delay	SW = 48 V and HS FET Turn-Off		36		
$t\_delay_{LS\_off}$	Low-Side Off Propagation Delay	SW = 0 V and LS FET Turn-Off		36		
t_match_{on}	Delay Matching LS_{off} to HS_{on}	LS Turn-Off to HS Turn-On		0		
t_match_{off}	Delay Matching HS_{off} to LS_{on}	HS Turn-Off to LS Turn-On		0		
t_lockout	Cross-conduction lockout time	LS turn-off to HS turn-on or HS turn-off to LS turn-on		5		
$t\_rise_{SW\_HS0}$	SW Rise Time at High Side FET Turn-On (Buck Mode, Hard Switching)	HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 5A		1		
$t\_rise_{SW\_HS1}$		HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 4.7 Ω, I_{LOAD} = 5A		3		
$t\_fall_{SW\_LS0}$	SW Fall Time at Low Side FET Turn-On (Boost Mode, Hard Switching)	LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV} = 0 Ω, I_{LOAD} = 5A		1		
$t\_fall_{SW\_LS1}$		LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV}= 4.7 Ω , I_{LOAD} = 5A		3		

(1) Parameters that show only a typical value are guaranteed by design and may not be tested in production

Electrical characteristics *(continued)*

Dynamic Characteristics Parameter Definition

Figure 3b: Logic Input to Output Switching Node Timing Diagram

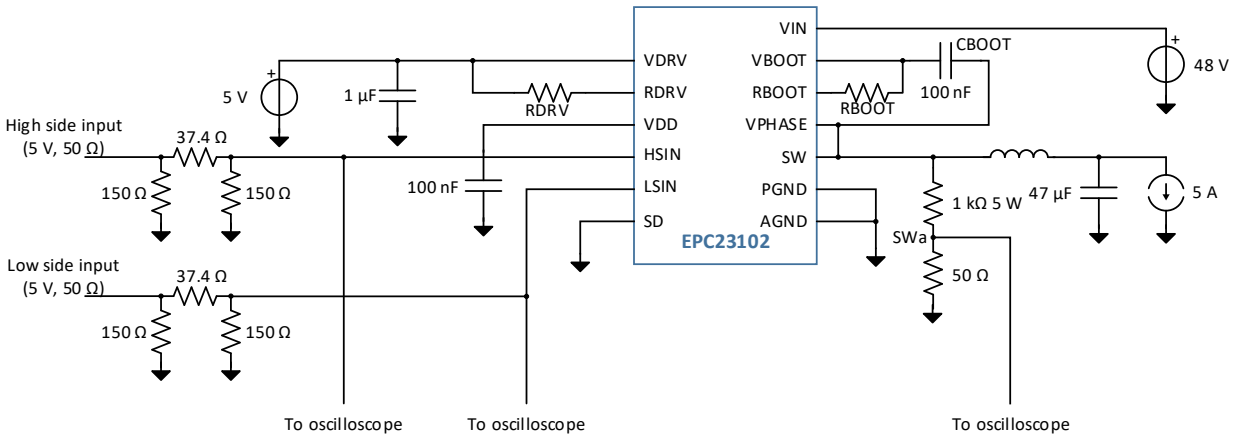
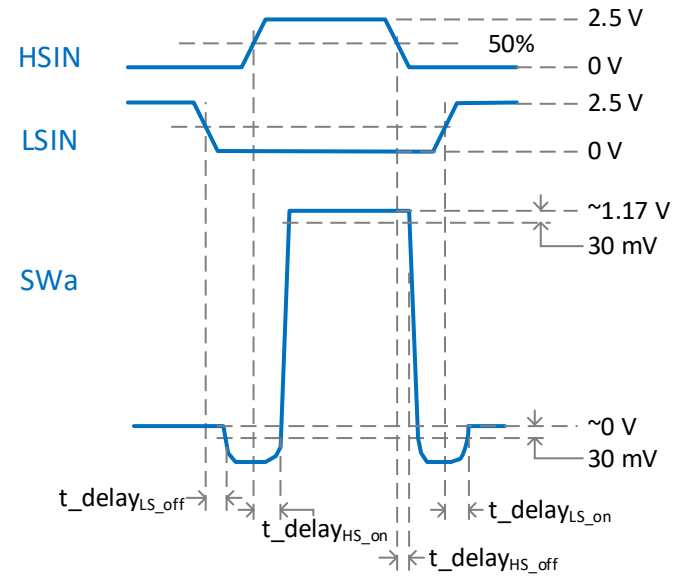


Figure 3b: Logic input to output switching node timing



Truth table

V_{DD}	$V_{BOOT} - V_{PHASE}$	HSIN	LSIN	HS FET	LS FET
$<V_{DD\_POR}$	–	–	–	OFF	OFF
$>V_{DD\_POR}$	$<V_{BOOT\_POR}$	–	0	OFF	OFF
		–	1	OFF	ON
$>V_{DD\_POR}$	$>V_{BOOT\_POR}$	0	0	OFF	OFF
		0	1	OFF	ON
		1	0	ON	OFF
		1	1	OFF	

Application information

General description

The EPC23102 ePower™ Stage IC integrates a half-bridge gate driver with internal high side and low side FETs. Integration is implemented using EPC's proprietary GaN IC technology. The monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits controlling high side and low side eGaN output FETs configured as a half-bridge power stage. Robust level shifters from low side to high side channels are designed to operate correctly with soft and hard switching conditions even at large negative clamped voltage and to avoid false trigger from fast dv/dt transients including those driven by external sources or other phases. Internal circuits integrate the functions of charging and disabling of the logic and bootstrap power supplies. Protection features are added to protect the output FETs from unwanted turn-on at low or even complete loss of supply voltages.

The single chip GaN IC is mounted inside a 3.5 x 5 mm Quad Flat No-lead (QFN) package using a flip chip on lead-frame technique. This packaging structure allows very low parasitic inductance from the power terminals to the underlying PCB solder pads. The exposed QFN pads are designed to have at least 0.6 mm spacing between high and low voltage pins to meet IPC voltage creepage rule for 100 V. Another enhancement exposes the backside of the Gan IC die on the top side of the package while completely encapsulating the rest of the GaN IC die. This allows a very low thermal resistance path from the die junction to an attached heatsink which in effect increases the allowable power dissipation and thus higher current handling capability.

Figure 4: Functional Block Diagram

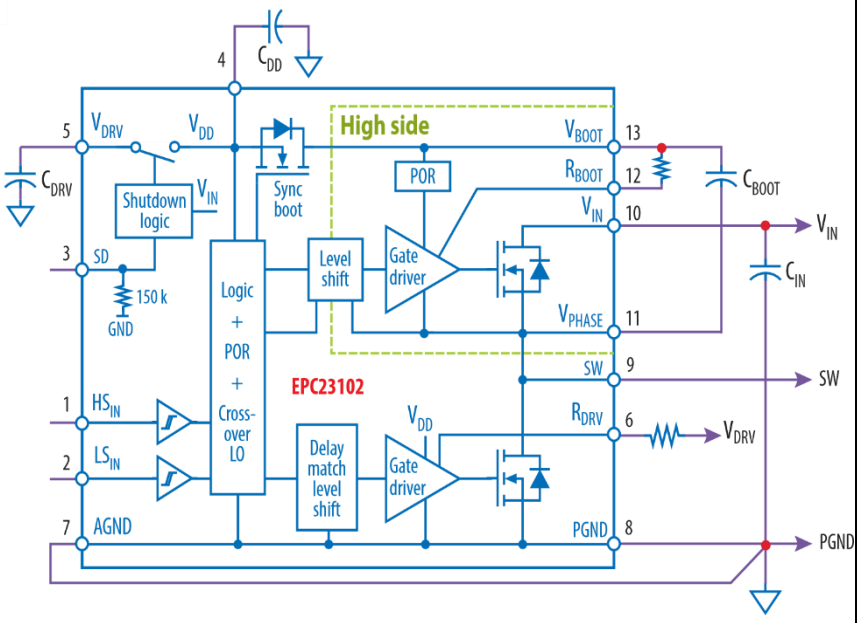
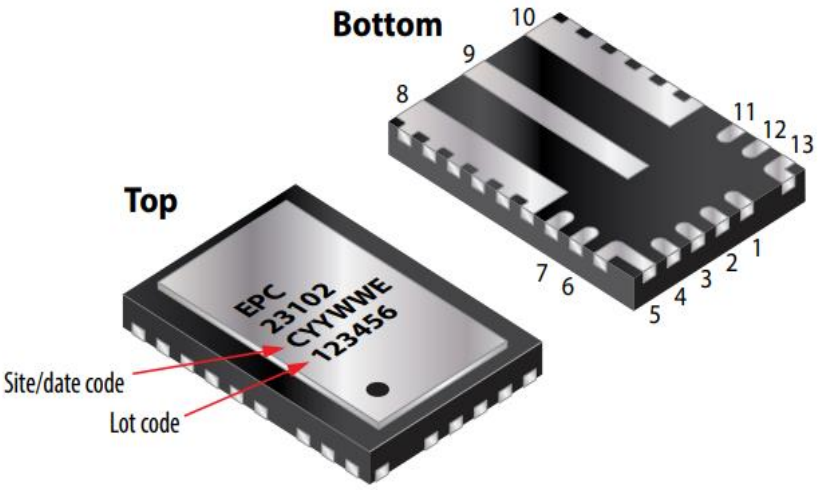


Figure 5: EPC23102 QFN package outline, pinouts and exposed backside of the GaN IC die



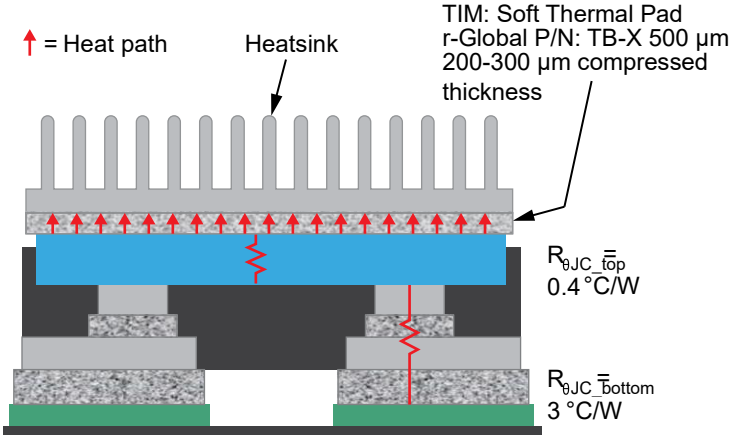
Output Current Rating

Power stage output current rating is best thought of as a figure of merit for specified output current level that accounts for the maximum amount of power dissipation allowed from the IC. Total power dissipation from a power stage IC is tied to the application circuit topologies, output current demand, switching frequencies, PCB construction, operating temperature range, thermal management technique and mechanical stress limit of the metallization imposed by electromigration. The rating is related to the respective maximum current capability of the two integrated output FETs in the half-bridge power stage but not measured the same way as individual discrete FET. For a power stage IC such as EPC23102, total power loss from the IC is the sum of the two output FETs conduction, switching and deadtime losses imposed by the application topologies at operating switching frequencies as well as power losses from the gate drive and logic circuit. The maximum power dissipation is defined by the following formula:

$$\text{Max } P_{Diss} = (\text{Max } T_J - T_A)/ R_{\theta JA}$$

where Max T_J is specified at 125 °C and the ambient temperature is specified at 25 °C. The big variable in achieving the theoretical maximum power dissipation is $R_{\theta JA}$, the thermal resistance from junction to ambient. The EPC23102 package construction allows two parallel path of heat dissipation where the bottom path goes from junction to metallization to lead-frame then the exposed pads at the bottom of the package. $R_{\theta JB\_bottom}$ is determined by the three power bars (VIN, SW and PGND) which are designed to allow maximum contact area to the underlying PCB pads. The total thermal resistance to ambient in this path of $R_{\theta JA\_bottom}$ needs to add the heat dissipation from the PCB pads through the multi-layer PCB construction then radiating to the ambient which is highly dependent on the airflow and forced cooling method. (See Figure 6).

Figure 6: Parallel Thermal Resistance Paths of EPC23102 IC from junction to ambient



To achieve even lower effective thermal resistance, another path is provided from junction to the relatively lower thermal resistance Si substrate of the GaN IC structure to the exposed backside of the entire die at the top of the package: $R_{\theta JC\_top}$ This lower thermal resistance path facilitates attachment of a topside heatsink through thermal interface material (TIM) to the exposed backside of the die. Note that the backside of the die is connected to the PGND (=AGND) pins which potentially provides added benefits of using electrically conductive TIM which has >2X higher thermal conductivity and lower cost than the insulating type. Typical parameters of electrically conducting vs. insulating TIMs are shown in the table below.

Typical parameters of electrically conducting vs. insulating TIMs		
Type of TIM	**Thermal Conductivity (W/m-K)**	**Relative Cost**
Electrically Conducting	40	1
Electrically Insulating	15	1.3

Another factor in specifying the output current rating is electromigration from a metallurgical standpoint. For EPC23102 this limit is a function of the metallization structure underlying the two output FETs plus their connection to the lead-frame and the three exposed power bars.

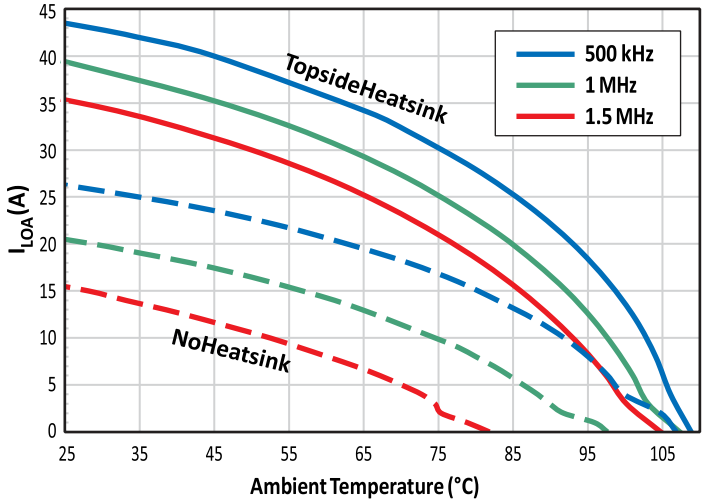
To provide real world test results, EPC uses a reference evaluation board, EPC90147 as shown in Figure 7, configured in a Buck Converter topology with the following test conditions: V_{IN} = 48 V, V_{OUT} = 12 V, PWM frequency = 0.5, 1, and 1.5 MHz, with and without top side heatsink, airflow = 500 and 1000 LFM, operating at ambient temperature starting at 25°C, maximum T_C not to exceed 110°C (derated from 125°C to avoid thermal runaway).

Figure 7: EPC90147 Evaluation Board (see EPC90147 Quick Start Guide for details)

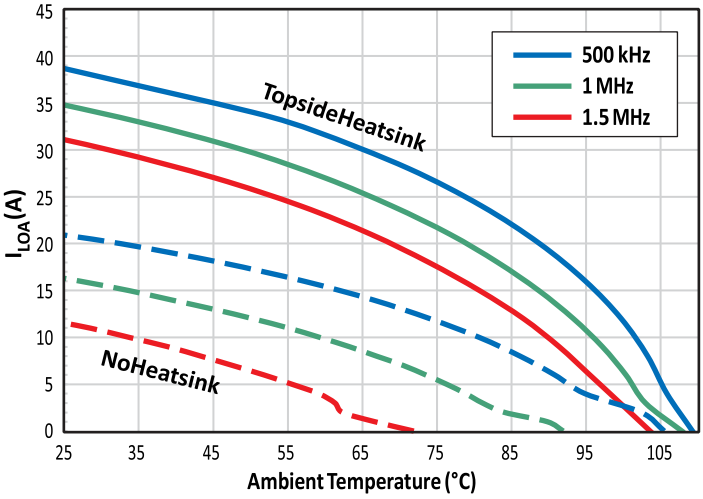
Thermal derating curves in Figure 8 are derived from measurement data. The difference between curves with top side heatsink (full lines) and without (dashed lines) show the dramatic difference of using the lower $R_{\theta JC\_top}$ of the higher thermal conductive path.

Figure 8: Thermal Derating Curves for Output Current Rating of EPC23102 IC using EPC90147 Evaluation Board

Airflow = 1000 LFM



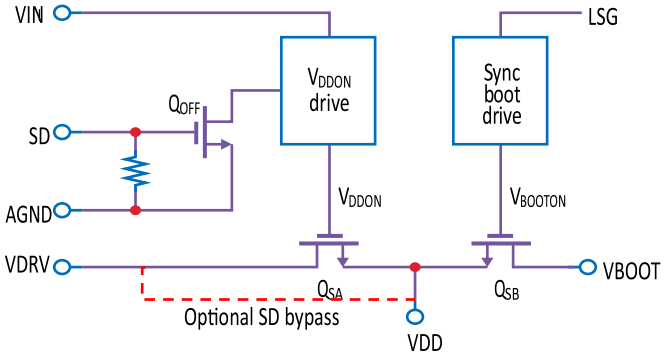
Airflow = 500 LFM



Power Supplies – V_{IN}, V_{DRV}, V_{DD}, and V_{BOOT}

The EPC23102 IC only requires an external 5 V VDRV power supply. Internal low side and high side power supplies, VDD and VBOOT, are generated from the external supply via two series connected switches. Figure 9 shows the simplified circuit diagram of the different power supplies inside the IC and their interaction with each other.

Figure 9: Simplified circuit diagram of VIN, VDRV, VDD, and VBOOT Power Supplies



The internal supplies can be disabled to save quiescent power by turning off the series switch, Q_{SA} in Figure 9, with 5 V applied to the SD pin to engage chip shutdown mode. In this mode, minimum current is drawn from the external VDRV supply while VDD is open circuit. Whatever charge remains within the VDD bypass capacitor will be discharged by the chip internal circuits by I_{DRV_Q}.

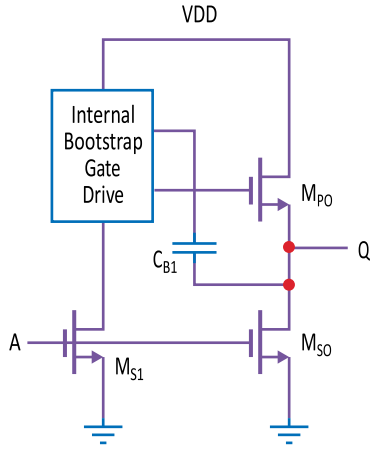
In the chip shutdown circuit, series switch (Q_{SA}) between VDRV and VDD is turned off by an internal shutdown circuit which itself derives its power from VIN such that the chip draws a current $I_{VIN\_disable}$ from VIN when shutdown mode is engaged. The SD function requires a minimum input voltage of $V_{IN,min}$ for the IC to be enabled. Below $VIN_{,min}$, the pass-transistor between VDRV and VDD will be off. To bypass the shutdown function, and thus extend the minimum operating voltage to $VIN\_no\_SD_{min}$, tie pins VDD and VDRV together.

The series connected high voltage synchronous bootstrap FET, Q_{SB} in Figure 9, between VDD and VBOOT for the high side floating bootstrap supply is activated only after the LS FET (Q2) is turned on to avoid overcharging during deadtime. The use of GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage is the lower dropout voltage of approximately 100 mV from the synchronous FET versus typical Si bootstrap diode voltage of 0.6 V. With synchronous charging VBOOT is maintained closer to the VDD voltage, allowing the HS FET gate drive circuit to have similar gate drive current and delay performance as the LS FET gate drive circuit.

Gate Driver

The EPC23102 IC integrates both HS and LS FET gate drivers with very low impedance and high pulse current push-pull NFET output stages. Figure 10 is the simplified circuit diagram of the gate driver output stage.

Figure 10: Simplified Circuit Diagram of Gate Driver Output Stage



The LS and HS gate drive voltage levels are derived from their respective internal low side (VDD) and high side (VBOOT) power supplies. To ensure that the gate drive level (Q) is sufficiently close to VDD or VBOOT, an internal bootstrap circuit is used to turn-on M_{PO}. Here the M_{PO} and M_{SO} pair works similarly to the half-bridge power stage Q1 and Q2 output FETs except all the circuits are internal to the IC. C_{B1} is an internal bootstrap capacitor. The PWM inputs, HSIN and LSIN, are used as the clocks for their respective high side and low side internal bootstrap gate drive circuit. As with any bootstrap circuit, the gate drive output cannot have 100% duty cycle to allow C_{B1} to be recharged. The PWM input pulse width must not exceed a maximum of PW_max on/off duration and a minimum pulse width on/off duration of PW_min as specified in the electrical characteristics table. At initial startup of the HSIN and LSIN clocking cycle, C_{B1} needs to be charged from zero. A delay of nominally 6 switching cycles appears before the gate drive output will follow the PWM input pulses. Figure 11a and 11b illustrate the gate drive output switching behavior.

SW Node Switching Transients

The switching rate and transients at the output node, SW, controlled by application topologies resulting in hard or soft switching transitions. The more stressful hard switching transition needs to be controlled by tuning the gate drive turn-on circuits for the HS FET (Q1) and LS FET (Q2) and minimizing the power loop parasitic inductances.

The on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Switching times are tuned by external resistors, R_{DRV} and R_{BOOT}, as shown in Figure 12 to achieve SW switching rates of 10 to 50 V/ns spanning zero to full load current. The choice of switching rates is dictated by efficiency versus EMI mitigation.

Figure 12: Simplified circuit diagram of external tuning resistor, internal gate drivers and output FETs

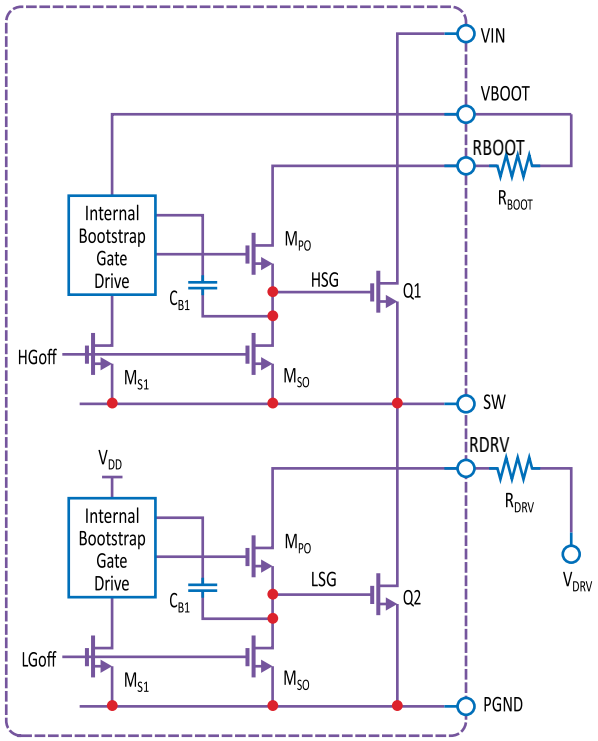


Figure 11a: Maximum and Minimum PWM Input Pulse Width On or Off duration to refresh internal gate drive bootstrap circuit

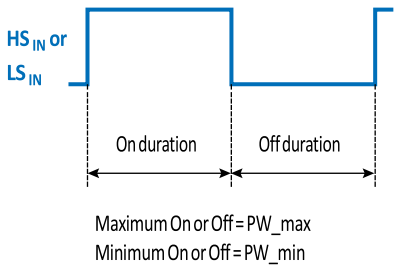
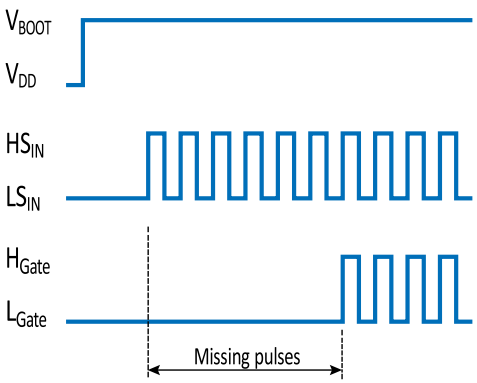


Figure 11b: Missing High Side and Low Side Gate pulses at startup due to initial charging of internal gate drive bootstrap circuit



During HS FET (Q1) or LS FET (Q2) turn-on transitions with hard switching conditions, the fast di/dt of the HS FET or LS FET coupled with the power loop inductance ($V_{peak} = L_{power\ loop} \cdot di/dt$) would cause a transient over- overvoltage spike on VIN or undervoltage spike on PGND. The EPC23102 pinouts for the three power bars (VIN, SW, PGND) are coupled with the design of optimal layout techniques to achieve minimized power loop inductance. Together with SW switching rate tuning by R_{DRV} and R_{BOOT}, the overvoltage spikes can be controlled to less than +10 V above rail and -10 V below ground during hard switching transitions.

The EPC90147 Evaluation Board provides guidelines for PCB layout to use the EPC23102 in application circuits together with the Gerber files and Bill of Material. To control SW switching rate and transients, 2.2 Ω are used for both R_{DRV} and R_{BOOT} for high frequency DC-DC converter switching around 1 MHz and 4.7 Ω used for 100 kHz motor drive inverter applications.

Protection Circuits

The EPC23102 integrates driver protection circuits as well as power on reset (POR) circuits for VDD and VBOOT. These protection circuits allow for the proper operation of the driver as shown in the Truth Table on page 6, regardless of the power-supply sequencing of VDRV with respect to VIN. This allows the system designer to use VIN to power-up VDRV without concerns on sequencing, as may be necessary in certain applications.

The Power On Reset (POR) circuit for the low side internal VDD supply will activate both the HS and LS logic paths when the VDD voltage rises above the rising threshold V_{DD_POR+}. The logic paths will become inactive when the VDD voltage falls by $V_{DD\_POR\_HYST}$ below the rising supply voltage threshold.

The Power On Reset (POR) circuit for the high side internal VBOOT supply will activate the HS driver path only when the bootstrap supply voltage, VBOOT, rises above the rising supply threshold of V_{BOOT_POR+}. The HS driver path will become inactive when the VBOOT bootstrap voltage falls by $V_{BOOT\_POR\_HYST}$ below the rising supply threshold.

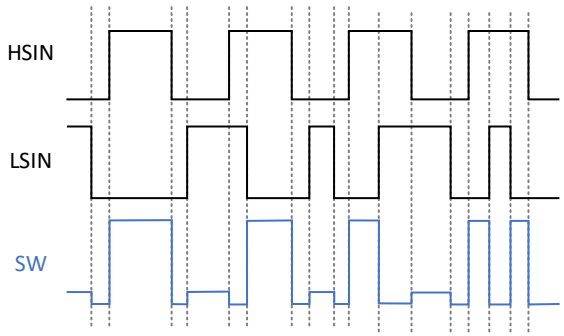
Logic Inputs

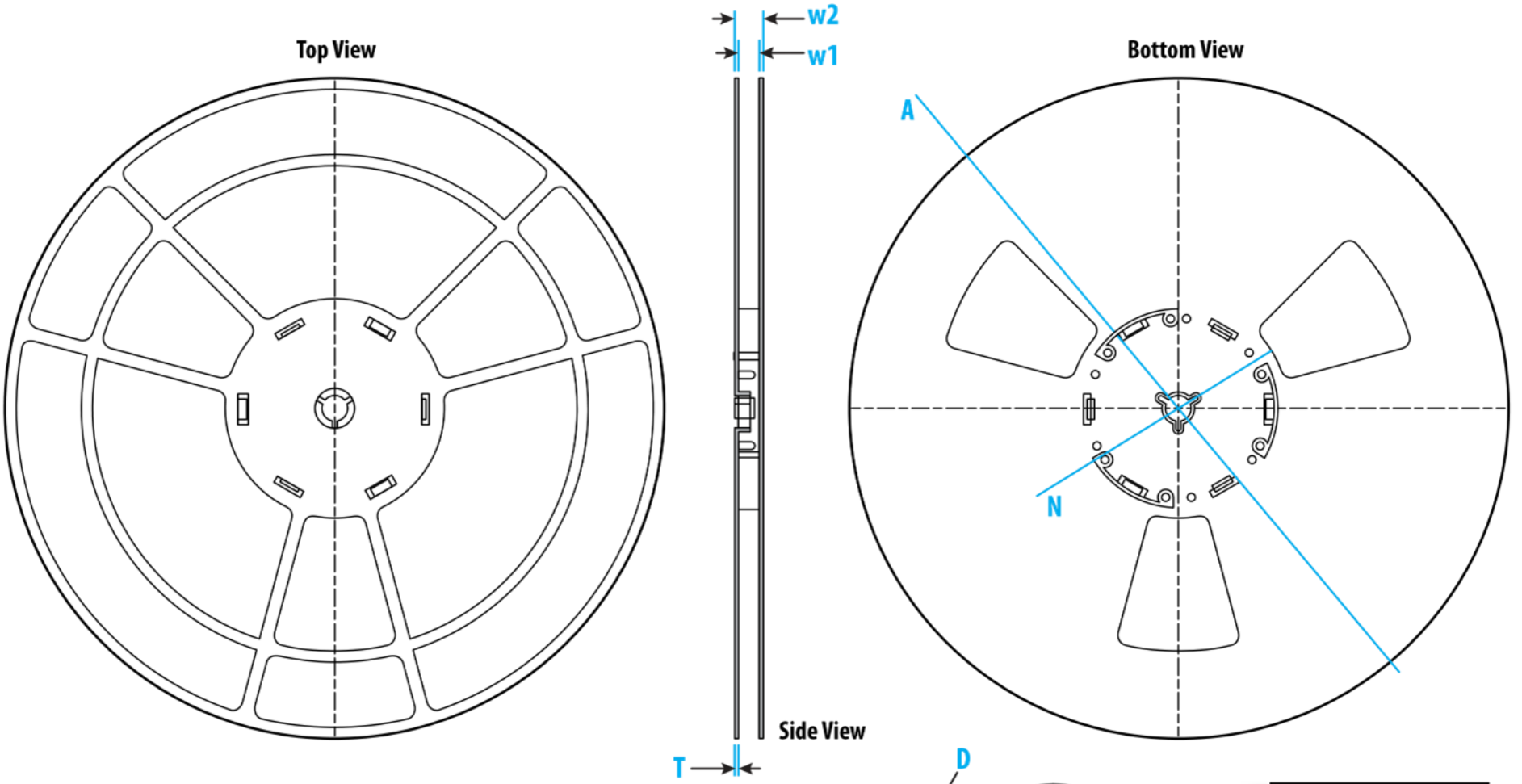
The EPC23102 IC is capable of interfacing to digital and analog controllers with 3.3 V or 5 V CMOS logic levels. The logic level-translator at the frontend level-shifts the PWM signals, HSIN and LSIN respectively, to internal voltage levels that allow for proper operation of the IC.

For interfacing with analog controllers that output a 12 V PWM signal, a resistor network in series should be inserted to divide the voltage to acceptable V_{IH} level and limit the input current into the logic input pins HSIN and LSIN which are clamped to the VDD supply by ESD protection network.

Separate and independent high side (HSIN) and low side (LSIN) logic control inputs allow external controllers to set fixed or adaptive deadtimes for optimal operating efficiency. Cross conduction lockout logic commands both FETs off when both logic inputs are simultaneously high. Figure 14 shows how the logic inputs interact with each other. Here the timing diagram applies with the HS FET (Q1) and LS FET (Q2) in half-bridge configuration and current is in the positive direction going out of the half-bridge. When HSIN and LSIN are logic high at same time, both Q1 and Q2 will shut off. A built-in lockout time of t_lockout is added, after which current then commutates to Q2 in 3rd quadrant conduction and SW will be clamped at negative V_{SD} voltage of Q2.

Figure 13: EPC23102 Input-to-Output Timing Diagram

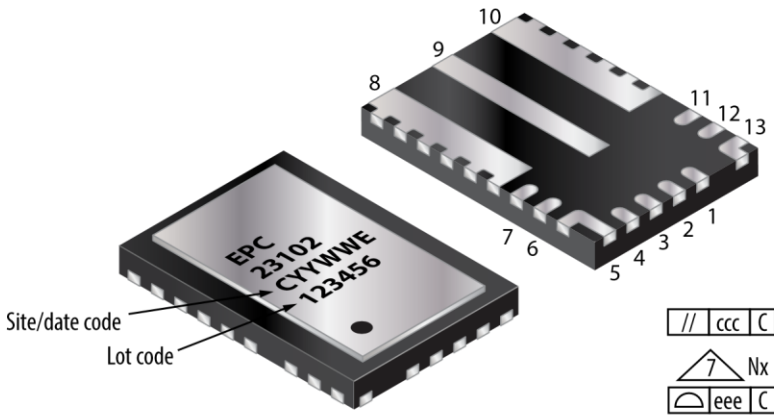




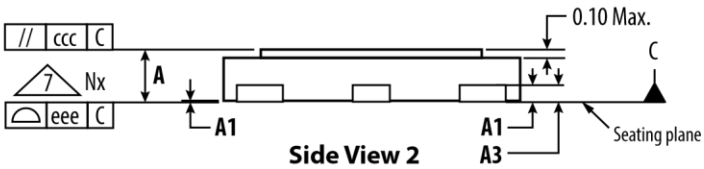
Top View Detail

Bottom View Detail

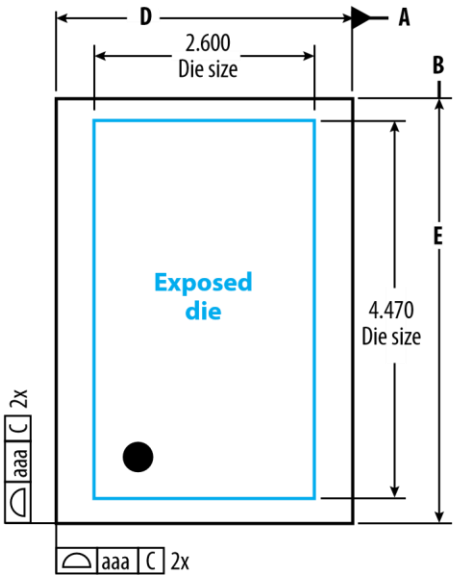
Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5



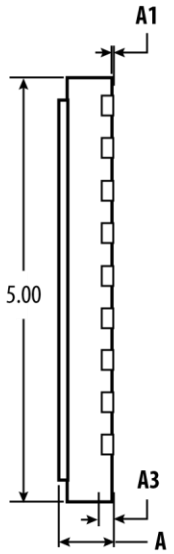
Pads 1-7, 11, 12 and 13 are IC pins
Pad 9 is a SW pin
Pad 8 is a PGND pin and 10 is a VIN pin



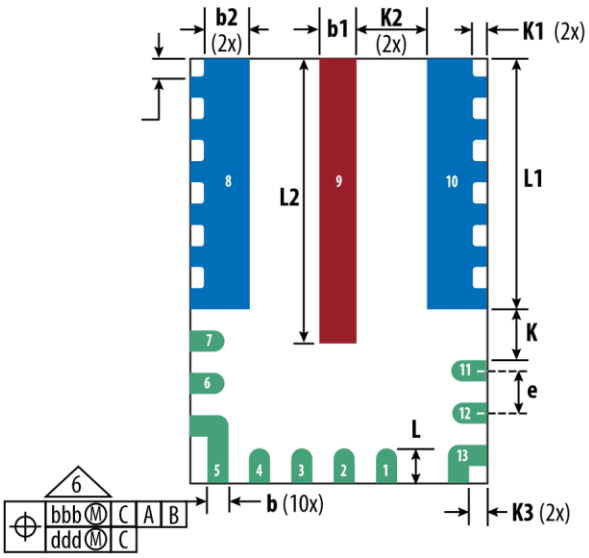
Side View 2



Top View



Side View 1



Bottom View

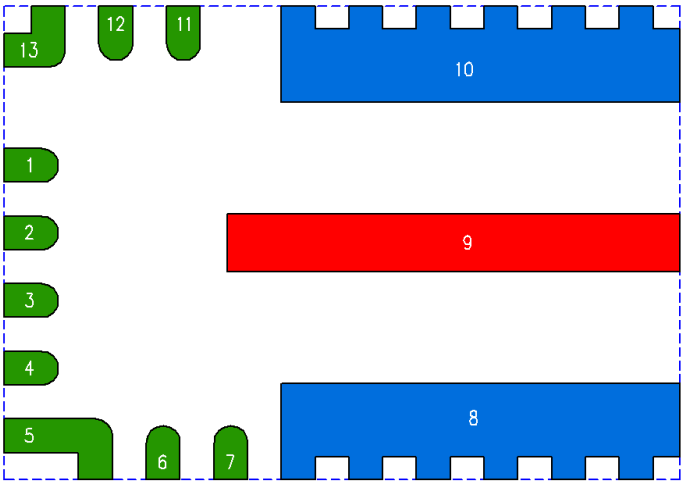
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	6
b1	0.38	0.43	0.48	6
b2	0.49	0.54	0.59	
D		3.50 BSC		
E		5.00 BSC		
e		0.50 BSC		
K	0.55	0.60	0.65	
K1	0.12	0.17	0.22	
K2	0.775	0.825	0.875	
K3	0.15	0.20	0.25	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
L	0.30	0.40	0.50	
L1	2.85	2.95	3.05	
L2	3.25	3.35	3.45	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		13		3
ND		6		5
NE		4		5
Notes		1, 2		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. **ND** and **NE** refer to the number of terminals on each **D** and **E** side respectively.
6. Dimension **b** applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
7. Coplanarity applies to the terminals and all the other bottom surface metallization.

Package (units in mm)
Transparent view

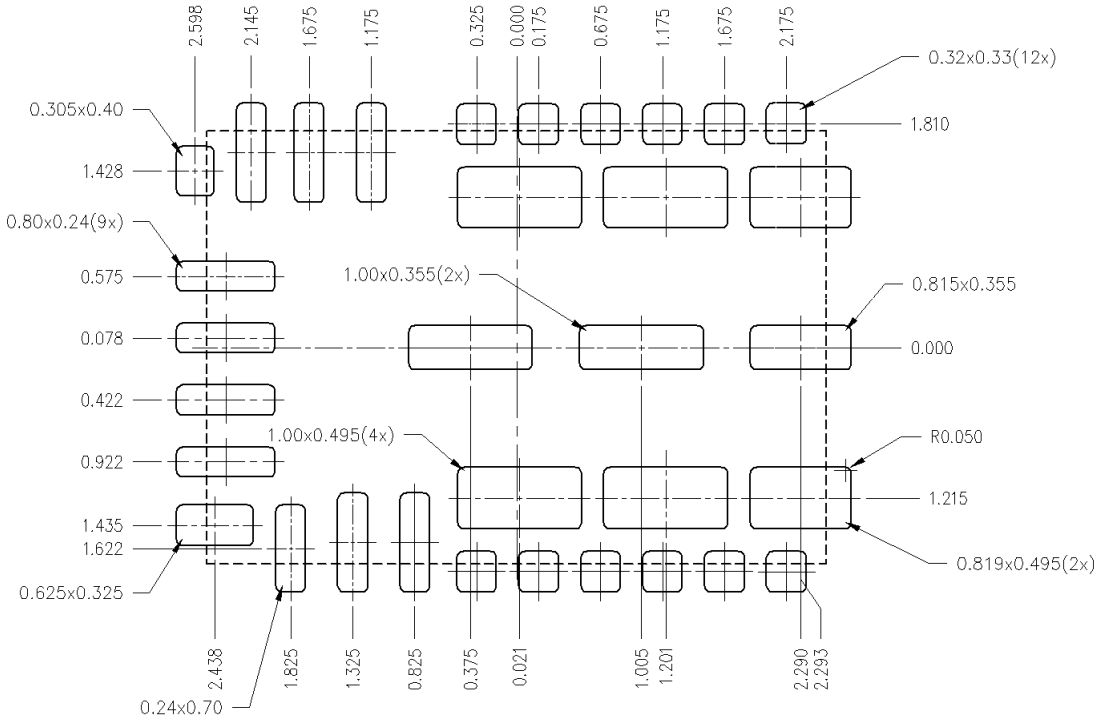


Pin	Description
1	HS_{IN}
2	LS_{IN}
3	SD
4	V_{DD}
5	V_{DRV}
6	R_{DRV}
7	AGND
8	PGND
9	SW
10	V_{IN}
11	V_{PHASE}
12	R_{BOOT}
13	V_{BOOT}

Recommended stencil (units in mm)

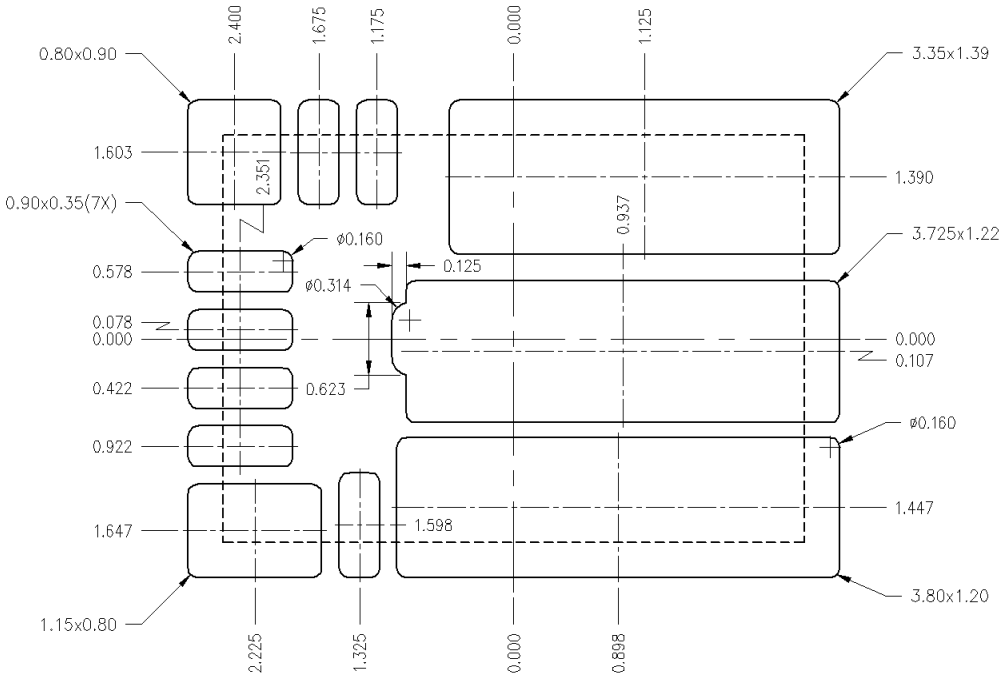
Recommended stencil should be 100 µm (4 mil) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

EPC has tested this stencil design and has not found any scooping issues.



Recommended copper layer (units in mm)

Copper layout provided as typical example layout.



Errata sheet

STATUS	VERSION	DATE	REMARK
ENGRT	2.0	4/19/2024	1. In boost mode feed-through operation, during non switching operation (both HS and LS OFF, or there is no VDD), the top GaN FET reverse conduction voltage drop may increase from 2V typical to >4V typical. A Schottky diode should be used across the top GaN FET if this operation mode is required.

Change log

STATUS	VERSION	DATE	REMARK
ENGRT	1.2	2/12/2024	• Update general template • Added boost mode operation details and limitations • Updated Protections section • Added $V_{IN\_no\_SD}$ parameter and description • Added $Ron_{\_SYNC\_BOOT}$ parameter • Updated switching loss conditions • Increased PW_MIN from 20ns to 30ns • Copper drawing fix • Modified Errata table
ENGRT	2.0	3/27/2024	• Updates $V_{IN\_no\_SD}$ parameter • Update t_delay • Update t_rise and t_fall for 0Ω • Remove all errata • Updated stencil dimensions and all drawings
		4/19/2024	• Added errata on boost mode operation