# EPC2619 – Enhancement Mode Power Transistor

$V_{DS}$ , 100 V

$R_{DS(on)}$ , 4.2 mΩ max

$I_D$ , 29 A

Pulsed $I_D$ , 164 A

**EPC** — EFFICIENT POWER CONVERSION

RoHS  Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

**Application Notes:**
- Easy-to-use and reliable gate
- Gate Drive ON = 5-5.25 V typical (negative voltage not needed)
- Recommended dead time (half-bridge circuit) ≤ 30 ns for best efficiency
- Top of FET is electrically connected to source

**Questions:**
**Ask a GaN Expert**

ASK AN EXPERT GaN
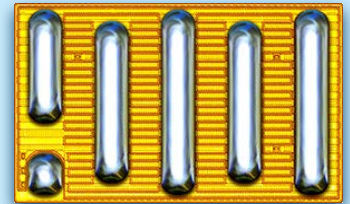
Die Size: 2.5 x 1.5 mm

**EPC2619** eGaN® FETs are supplied only in passivated die form with solder bars.

### Applications
- DC-DC Converters
- Isolated DC-DC Converters
- Sync Rectification
- Battery Chargers, Storage, and Stabilizers
- Solar Optimizers
- Motor Drive
- Power Tools
- eBikes and eScooters
- Robots
- DC Servo
- Medical Robots and DC-DC
- Class D Audio
- USB PD 3.1 Chargers
- Point of Load Converters

### Benefits
- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low $Q_G$
- Small Footprint
- Excellent Thermal

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2619

| Maximum Ratings | | | |
|---|---|---|---|
| **PARAMETER** | | **VALUE** | **UNIT** |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 100 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C) | 120 | |
| $I_D$ | Continuous ($T_A$ = 25°C) | 29 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 164 | |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| **PARAMETER** | | **TYP** | **UNIT** |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Case TOP) | 1 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board (Case BOTTOM) | 2.6 | |
| $R_{\theta JA\_JEDEC}$ | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB) | 66 | |
| $R_{\theta JA\_EVB}$ | Thermal Resistance, Junction-to-Ambient (EPC90153 EVB) | 46 | |

| Static Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 100 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{GS}$ = 0 V, $V_{DS}$ = 80 V | | 0.01 | 0.1 | mA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.02 | 1.6 | |
| | Gate-to-Source Forward Leakage# | $V_{GS}$ = 5 V, $T_J$ = 125°C | | 0.05 | 3.6 | |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 0.007 | 1 | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 5.5 mA | 0.8 | 1.1 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 16 A | | 3.3 | 4.2 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage# | $I_S$ = 0.5 A, $V_{GS}$ = 0 V | | 1.6 | | V |

\# Defined by design. Not subject to production test.

| Dynamic Characteristics# ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 1180 | 1570 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 3.0 | | |
| $C_{OSS}$ | Output Capacitance | | | 350 | 470 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS}$ = 0 to 50 V, $V_{GS}$ = 0 V | | 400 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 530 | | |
| $R_G$ | Gate Resistance | | | 0.4 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 16 A | | 8.5 | 10.3 | nC |
| $Q_{GS}$ | Gate-to-Source Charge | | | 2.2 | | |
| $Q_{GD}$ | Gate-to-Drain Charge | $V_{DS}$ = 50 V, $I_D$ = 16 A | | 1.0 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 1.6 | | |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 27 | 31 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

\# Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50 V.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50 V.

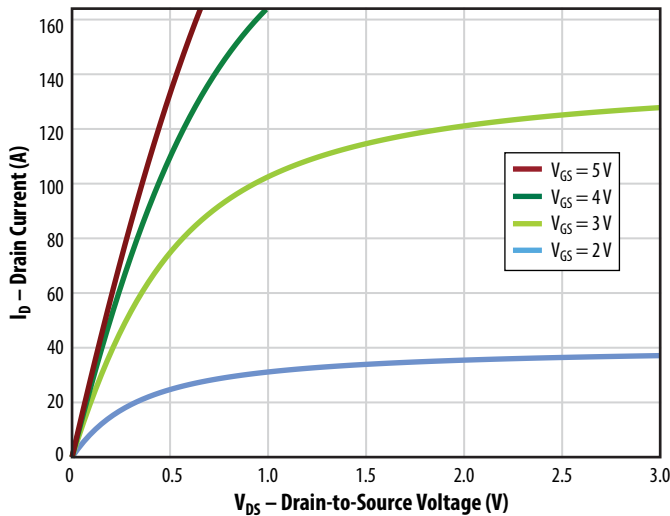### Figure 1: Typical Output Characteristics at 25°C
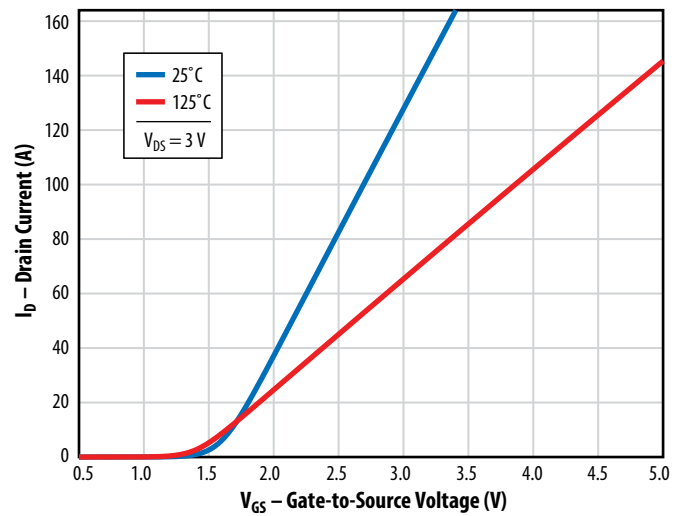


### Figure 2: Typical Transfer Characteristics



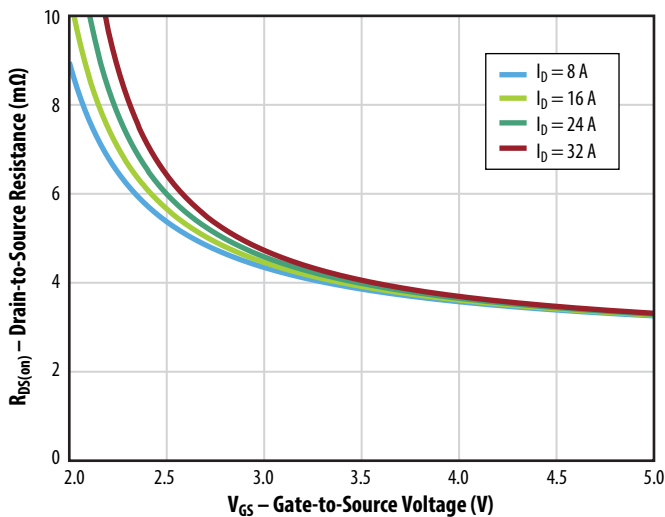### Figure 3: $R_{DS(on)}$ vs. $V_{GS}$ for Various Drain Currents



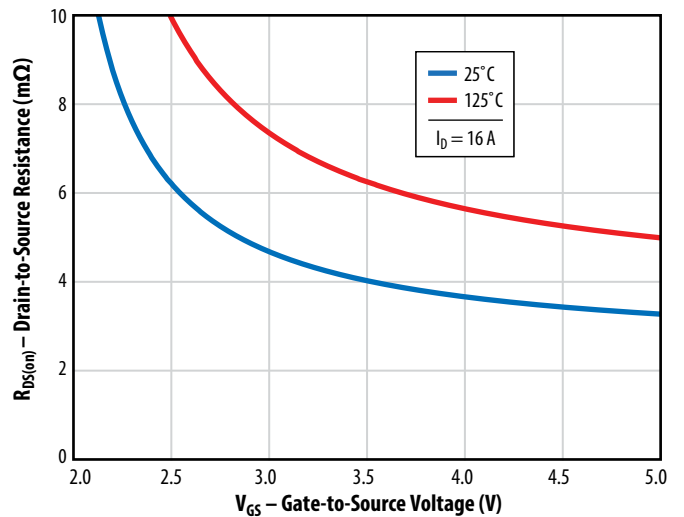### Figure 4: Typical $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures
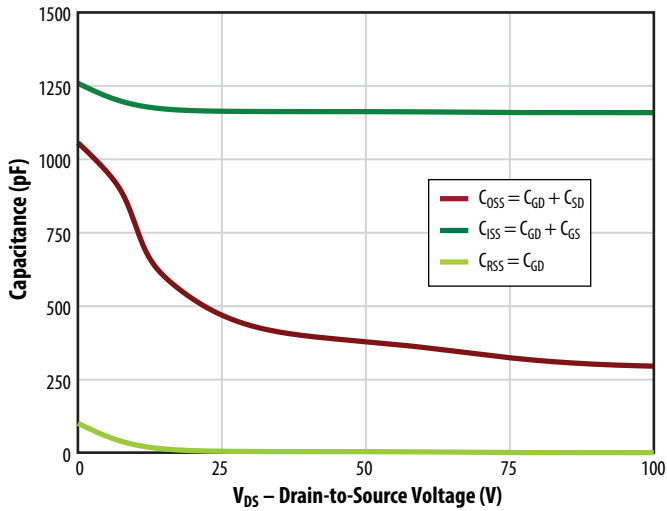
**Figure 5a: Typical Capacitance (Linear Scale)**

Capacitance (pF) vs $V_{DS}$ – Drain-to-Source Voltage (V)
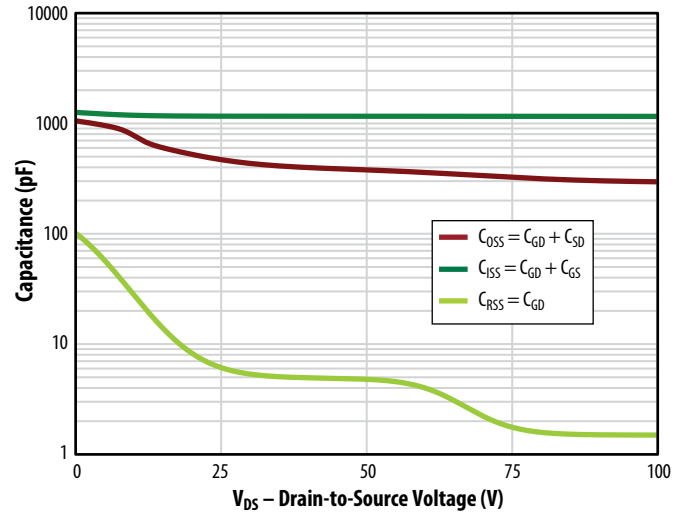
$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

**Figure 5b: Typical Capacitance (Log Scale)**

Capacitance (pF) vs $V_{DS}$ – Drain-to-Source Voltage (V)

$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

**Figure 6: Typical Output Charge and C$_{OSS}$ Stored Energy**

$Q_{OSS}$ – Output Charge (nC) / $E_{OSS}$ – $C_{OSS}$ Stored Energy (µJ) vs $V_{DS}$ – Drain-to-Source Voltage (V)
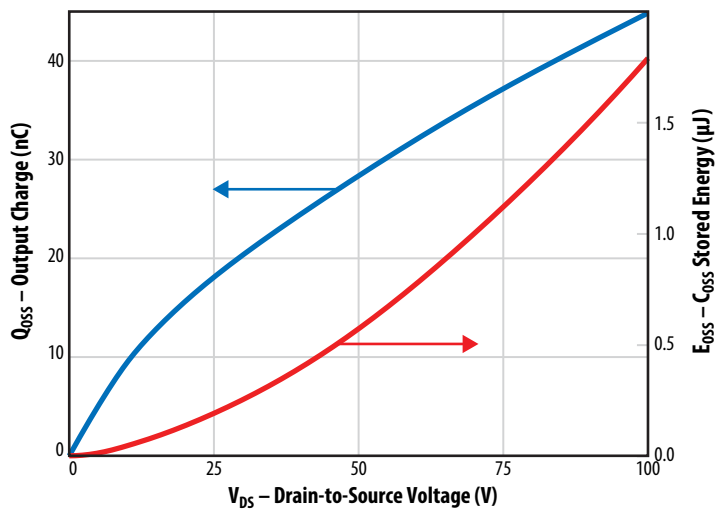
**Figure 7: Typical Gate Charge**

$V_{GS}$ – Gate-to-Source Voltage (V) vs $Q_G$ – Gate Charge (nC)

$I_D = 16$ A
$V_{DS} = 50$ V
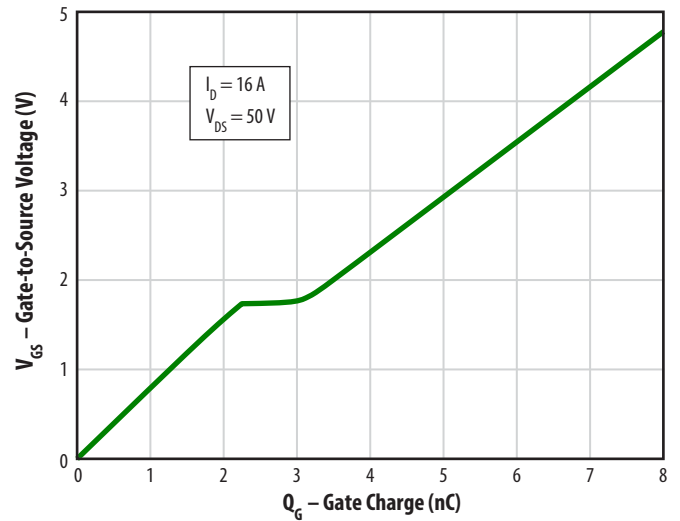
**Figure 8: Reverse Drain-Source Characteristics**

$I_{SD}$ – Source-to-Drain Current (A) vs $V_{SD}$ – Source-to-Drain Voltage (V)

25°C
125°C
$V_{GS} = 0$ V
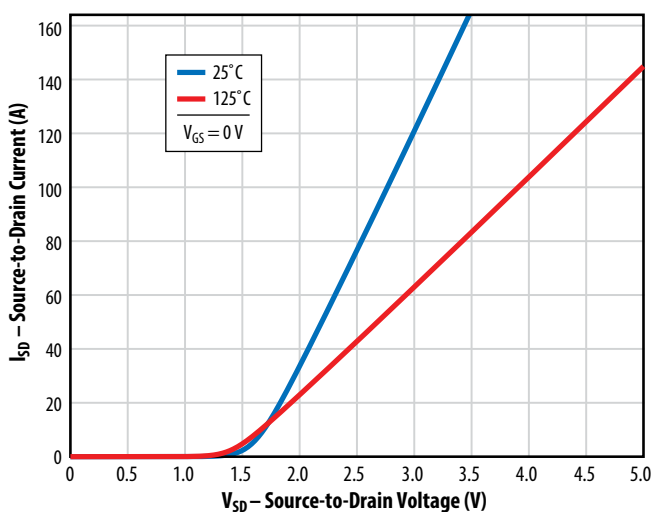
**Figure 9: Normalized On-State Resistance vs. Temperature**

Normalized On-State Resistance $R_{DS(on)}$ vs $T_J$ – Junction Temperature (°C)

$I_D = 16$ A
$V_{GS} = 5$ V
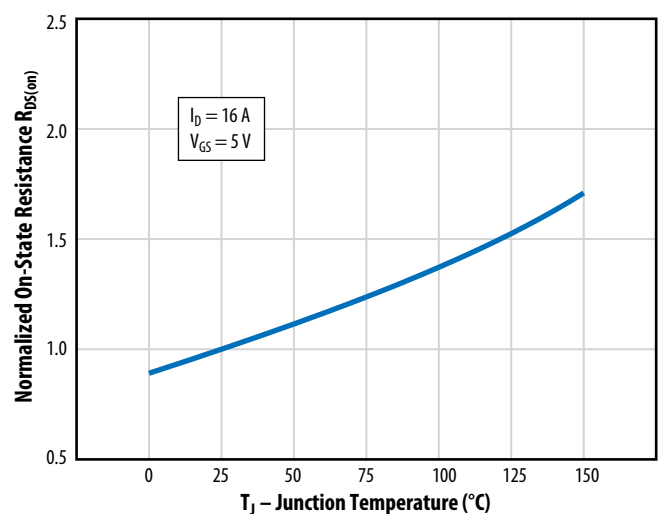
**Note:** Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

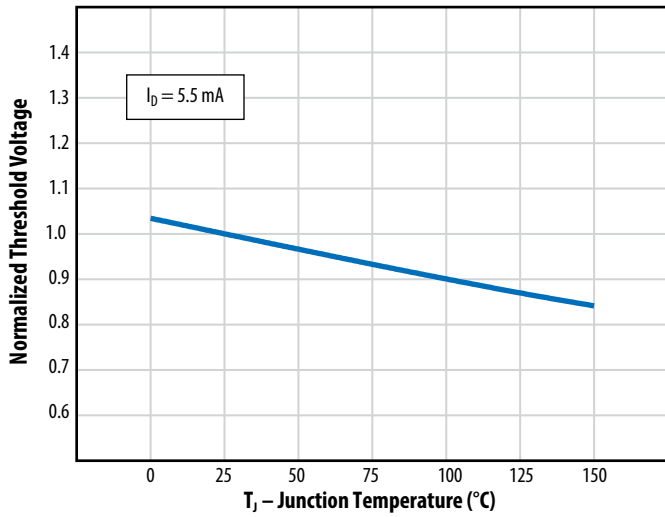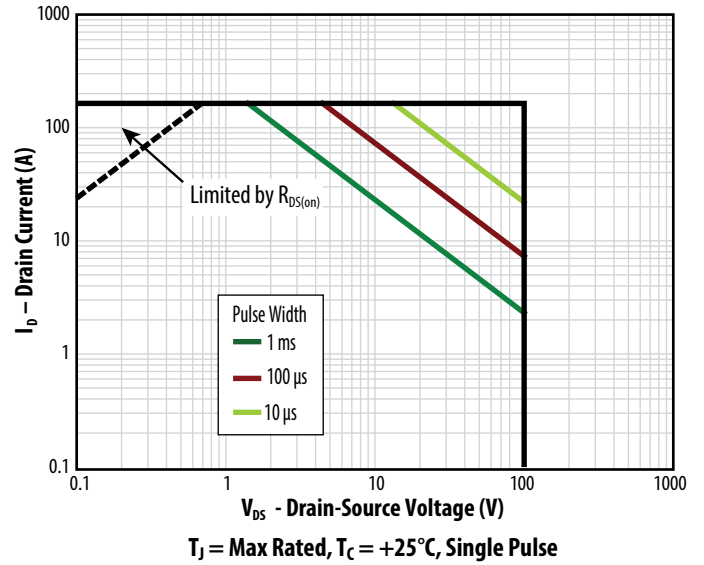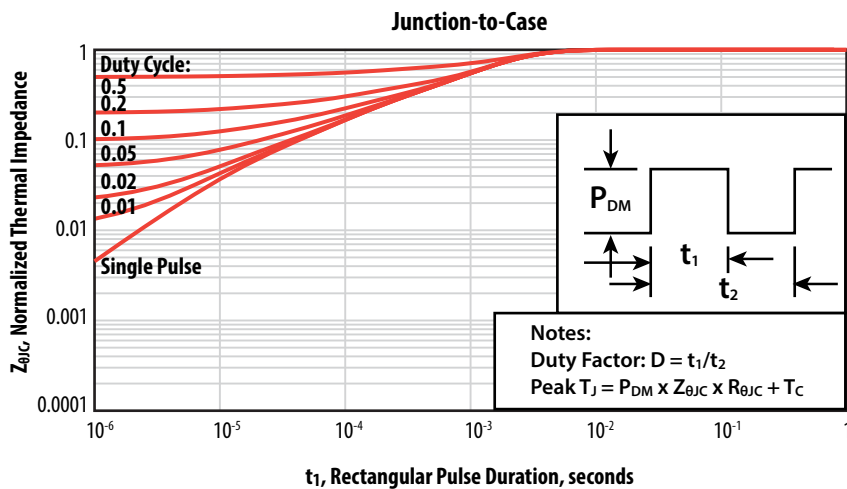**Figure 10: Normalized Threshold Voltage vs. Temperature**



$I_D = 5.5$ mA

Y-axis: Normalized Threshold Voltage
X-axis: $T_J$ – Junction Temperature (°C)

**Figure 11: Safe Operating Area**



Limited by $R_{DS(on)}$

Pulse Width
- 1 ms
- 100 µs
- 10 µs

Y-axis: $I_D$ – Drain Current (A)
X-axis: $V_{DS}$ - Drain-Source Voltage (V)

$T_J$ = Max Rated, $T_C$ = +25°C, Single Pulse

**Figure 12:  Transient Thermal Response Curves**

**Junction-to-Board**



Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

Y-axis: $Z_{\theta JB}$, Normalized Thermal Impedance
X-axis: $t_1$, Rectangular Pulse Duration, seconds

$P_{DM}$
$t_1$
$t_2$

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM}$ x $Z_{\theta JB}$ x $R_{\theta JB} + T_B$

**Junction-to-Case**



Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

Y-axis: $Z_{\theta JC}$, Normalized Thermal Impedance
X-axis: $t_1$, Rectangular Pulse Duration, seconds

$P_{DM}$
$t_1$
$t_2$

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM}$ x $Z_{\theta JC}$ x $R_{\theta JC} + T_C$

## LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout consider-ations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The **EPC90153 80 V Half-bridge with Gate Drive using EPC2619** implements our recommended vertical inner layout.
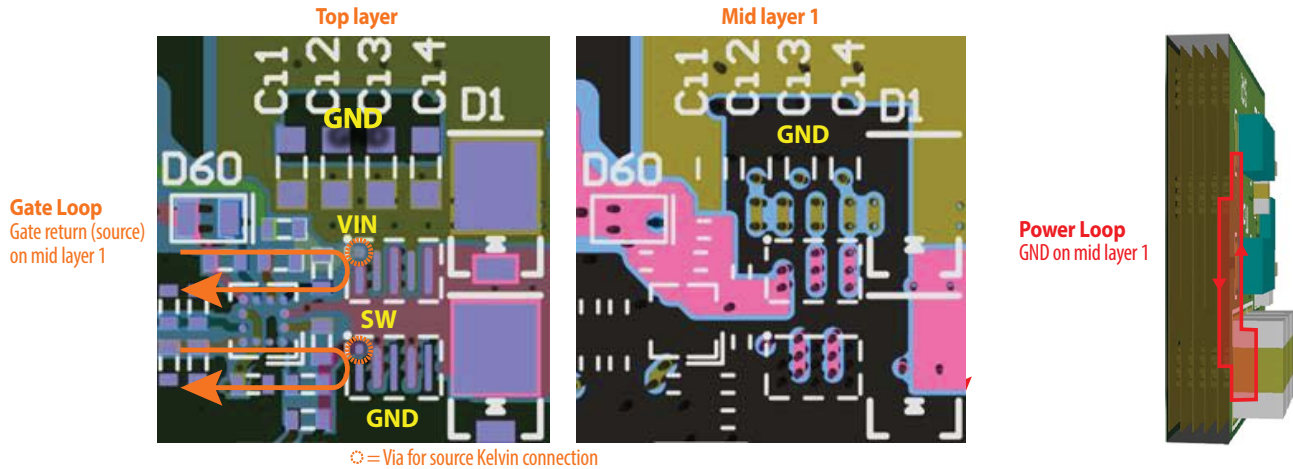


*Figure 13: Inner vertical layout for power and gate loops from EPC9097*

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**
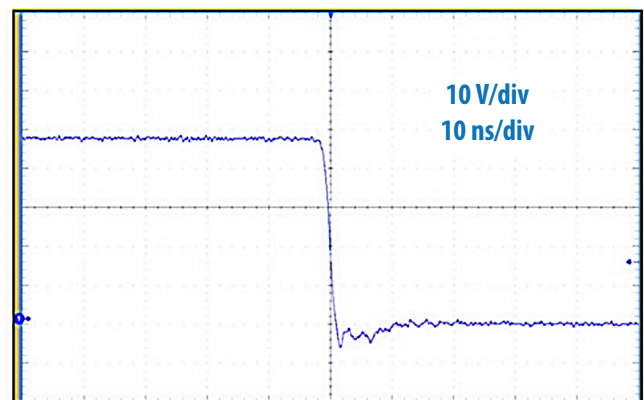
## TYPICAL SWITCHING BEHAVIOR

The following typical switching waveforms are captured in these conditions:

- **EPC90153 80 V Half-bridge with Gate Drive using EPC2619**
- Gate driver: uP1966E with 0.4 Ω/0.7 Ω pull-down/pull-up resistance
- External $R_G$(ON) = 1.8 Ω, $R_G$(OFF) = 0.47 Ω
- $V_{IN}$ = 48 V, $I_L$ = 20 A
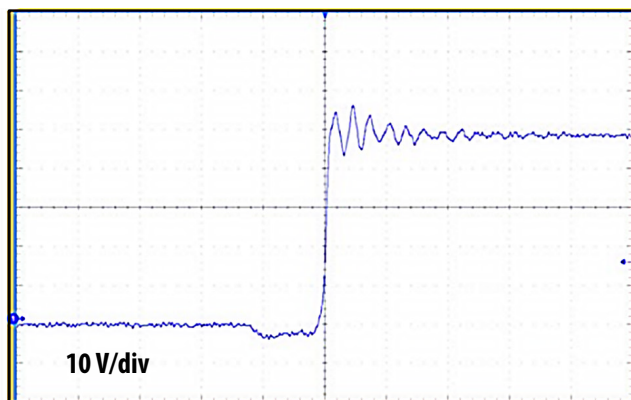


**Typical turn on: 47 V/ns**

**Typical turn off: 22 V/ns**

*Figure 14: Typical half-bridge voltage switching waveforms*

See the **EPC90153 80 V Half-bridge with Gate Drive using EPC2619 Quick Start Guide** for more information.

## TYPICAL THERMAL CONCEPT

The EPC2204 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. *Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM)  needs to provide electrical isolation to the heatsink.*

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.
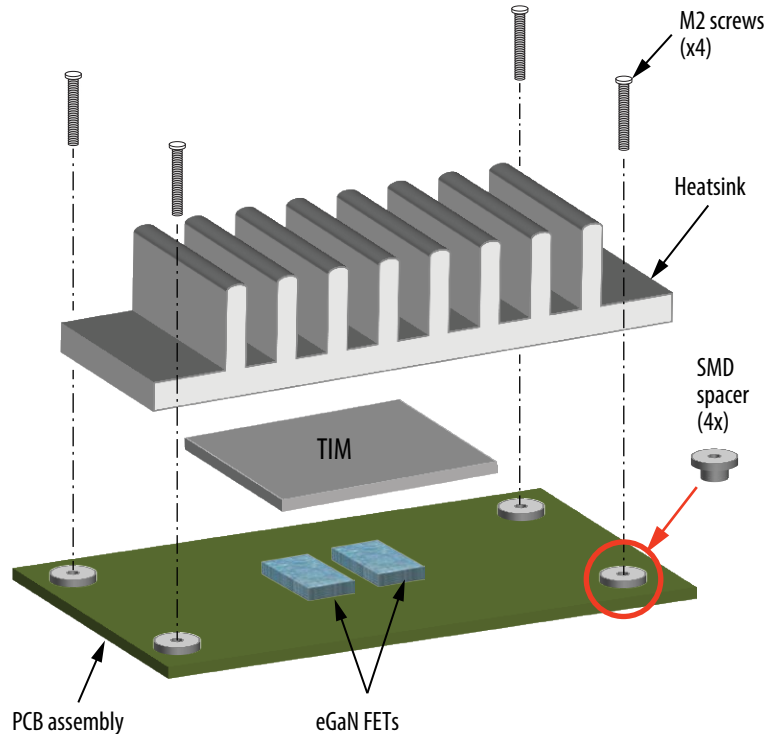


*Figure 15: Exploded view of heatsink assembly using screws*
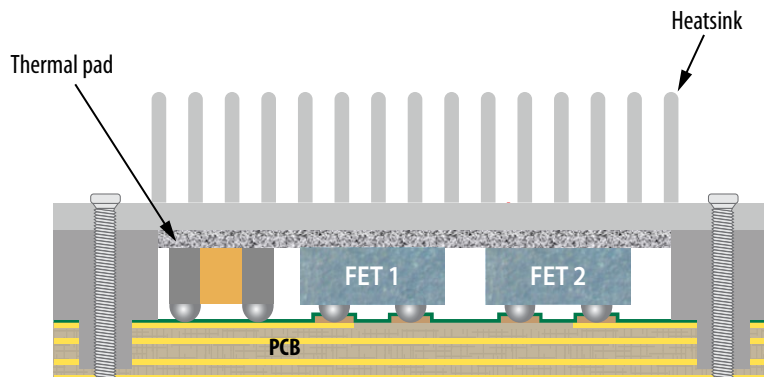


*Figure 16: A cross-section image of dual sided thermal solution*

**Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI**

The thermal design can be optimized by using the *GaN FET Thermal Calculator* on EPC's website.

## TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

7" inch reel
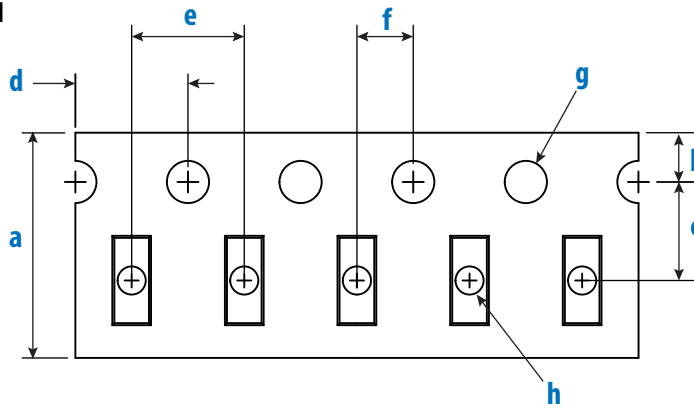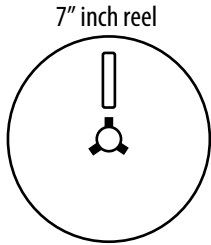
Loaded Tape Feed Direction ⇨

Die orientation dot

ZZZZ
YYYY
2619

Gate solder bar is under this corner

Die is placed into pocket solder bar side down (face side down)

| EPC2619 (Note 1) | Dimension (mm) | | |
|---|---|---|---|
| | Target | MIN | MAX |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |
| h | 0.50 | 0.45 | 0.55 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

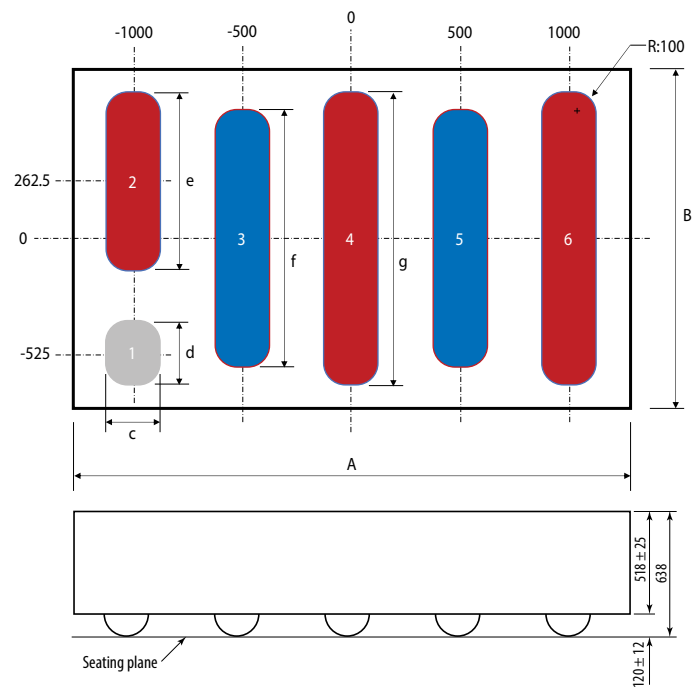Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

## DIE MARKINGS

2619
YYYY
ZZZZ

Die orientation dot

Gate Pad bar is under this corner
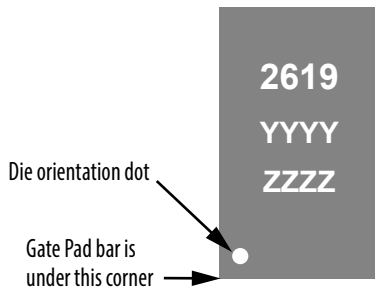
| Part Number | Laser Markings | | |
|---|---|---|---|
| | Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC2619 | 2619 | YYYY | ZZZZ |

## DIE OUTLINE

Solder Bump View

R:100

| DIM | Micrometers | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 2470 | 2500 | 2530 |
| B | 1470 | 1500 | 1530 |
| c | | 250 | |
| d | | 300 | |
| e | | 825 | |
| f | | 1175 | |
| g | | 1350 | |

**Pad 1 is Gate;**

**Pads 2 ,4, 6 are Source;**

**Pads 3, 5 are Drain**

Side View

518 ± 25

638

120 ± 12

Seating plane

**RECOMMENDED LAND PATTERN**
*(units in µm)*
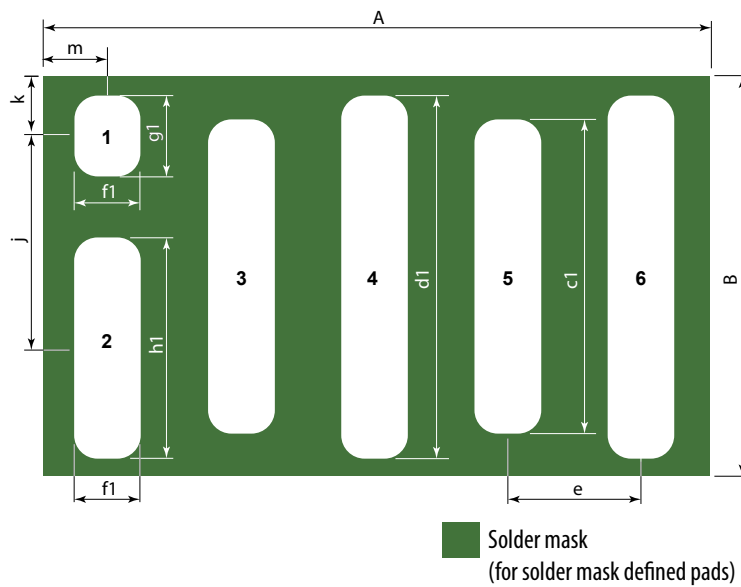


| DIM | Nominal |
|-----|---------|
| A | 2500 |
| B | 1500 |
| c1 | 1155 |
| d1 | 1330 |
| e | 500 |
| f1 | 230 |
| g1 | 280 |
| h1 | 805 |
| j | 787.5 |
| k | 225 |
| m | 250 |

Pad 1 is Gate;
Pads 2, 4, 6 are Source;
Pads 3, 5 are Drain

Solder mask
(for solder mask defined pads)

**RECOMMENDED STENCIL DRAWING**
*(units in µm)*
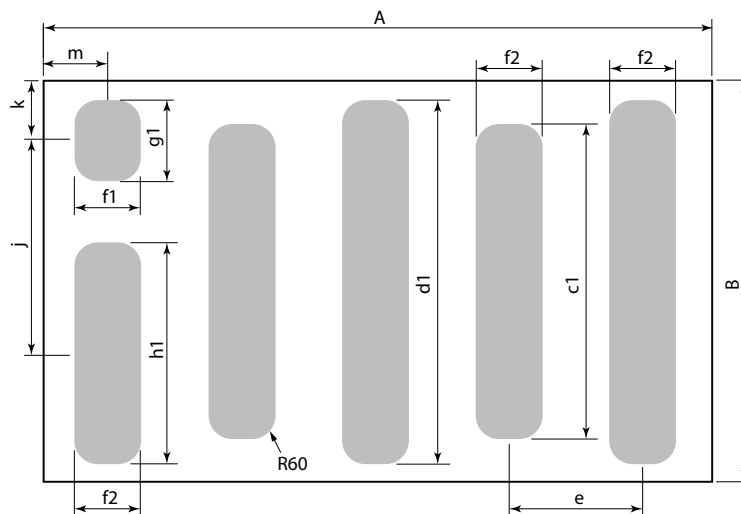


| DIM | Nominal |
|-----|---------|
| A | 2500 |
| B | 1500 |
| c1 | 1155 |
| d1 | 1330 |
| e | 500 |
| f1 | 230 |
| f2 | 210 |
| g1 | 280 |
| h1 | 805 |
| j | 787.5 |
| k | 225 |
| m | 250 |

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

## ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.
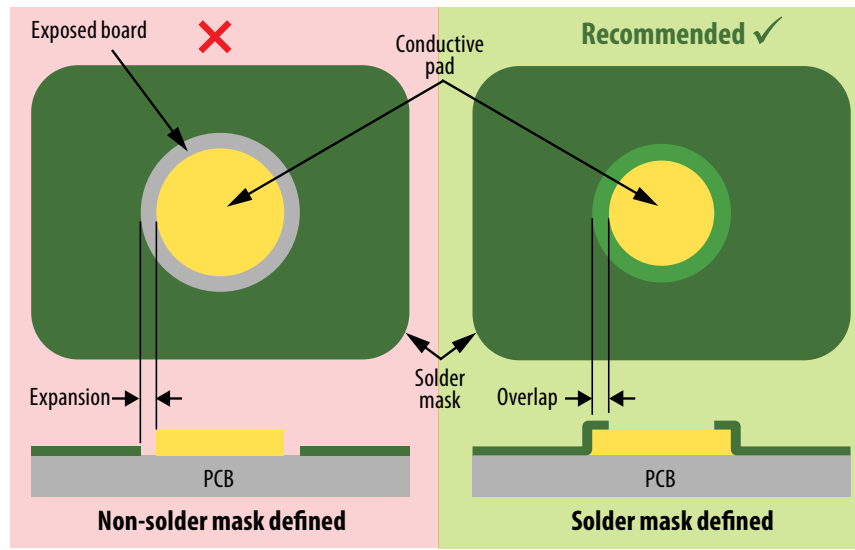


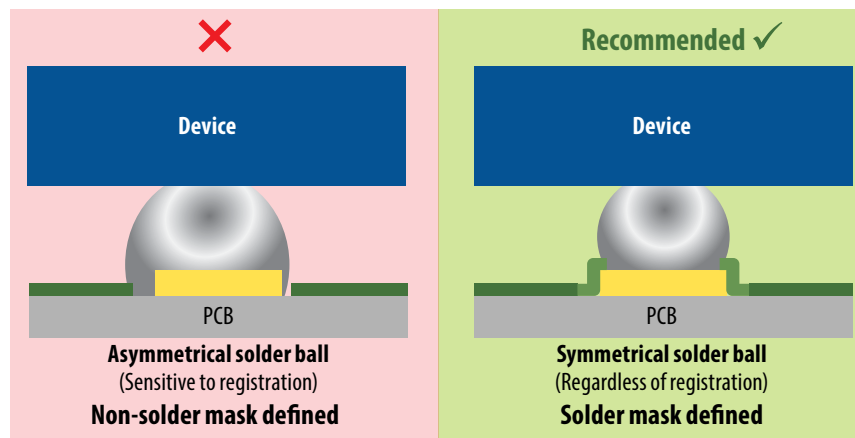*Figure 17: Solder mask defined versus non-solder mask defined pad*



*Figure 18: Effect of solder mask design on the solder ball symmetry*

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip**
  (for preliminary device Altium footprints, contact EPC)