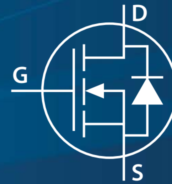
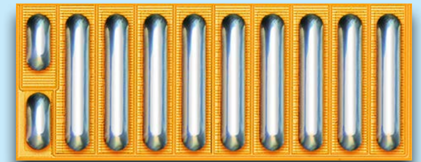
EPC2901C_55 – Enhancement Mode Power Transistor

V_{DS}, 100 V
$R_{DS(on)}$, 7 mΩ max
I_D, 36 A
95% Pb/5% Sn Solder



Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2901C_55 eGaN® FETs are supplied only in passivated die form with solder bars

Applications
- High-Frequency DC-DC Conversion
- Industrial Automation
- Synchronous Rectification
- Low Inductance Motor Drives

Benefits
- Ultra High Efficiency
- Ultra Low Switching and Conduction Losses
- Zero Q_{RR}
- Ultra Small Footprint

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C, $R_{θJA}$ = 7.3)	36	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	150	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	2	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	54	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)

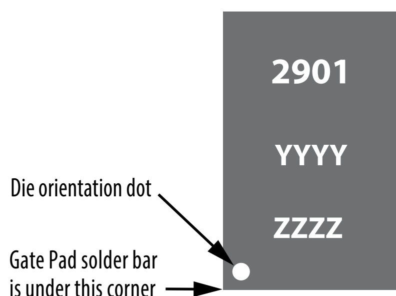
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		2	250	µA
		V_{GS} = 0 V, V_{DS} = 80 V, T_J = -55°C		0.9	50	
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.019	2	mA
		V_{GS} = 5 V, T_J = -55°C		0.01	1.5	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		1.4	250	µA
		V_{GS} = -4 V, T_J = -55°C		0.14	50	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5 mA	0.8	1.6	2.5	V
		V_{DS} = V_{GS}, I_D = 5 mA, T_J = -55°C		1.7	2.7	
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A		4.8	7	mΩ
		V_{GS} = 5 V, I_D = 25 A, T_J = -55°C		3.1	6.5	
V_{SD}	Source-to-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.8		V

All measurements were done with substrate connected to source
Defined by design. Not subject to production test

Dynamic Characteristics #(T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		756	1020	pF
C_{RSS}	Reverse Transfer Capacitance			9.25	13	
C_{OSS}	Output Capacitance			493	650	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related			567		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related			711		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 25 A		6.9	10	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 50 V, I_D = 25 A		1.9		
Q_{GD}	Gate to Drain Charge			1.35	2	
$Q_{G(TH)}$	Gate Charge at Threshold			1.2		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		36	45	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source
Defined by design. Not subject to production test

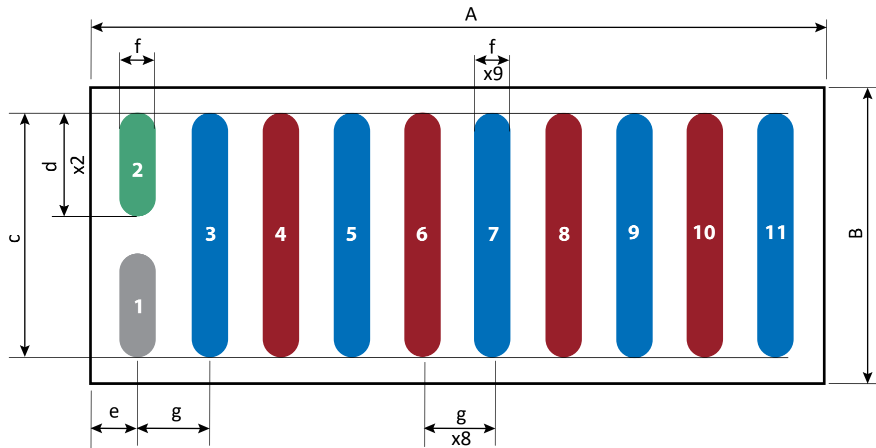
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2901C_55	2901	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View

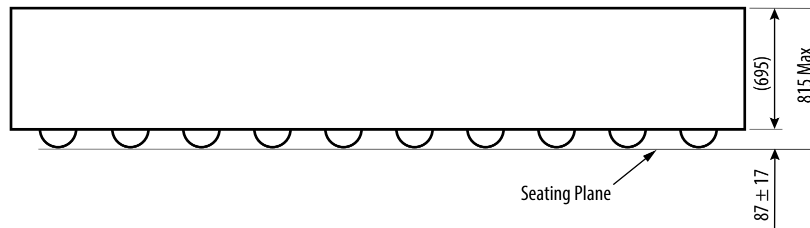


DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1605	1635	1665
c	1362	1382	1402
d	560	580	600
e	235	250	265
f	180	200	220
g		400	

Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.*

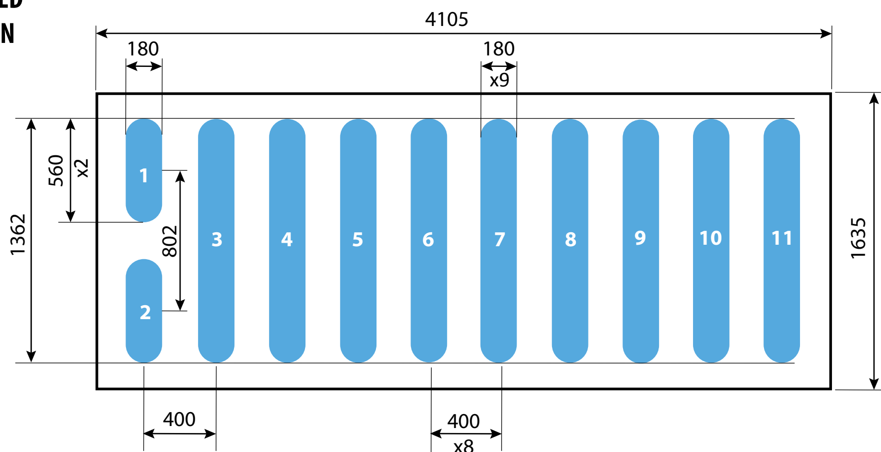
*Substrate pin should be connected to Source

Side View



RECOMMENDED LAND PATTERN

(units in µm)



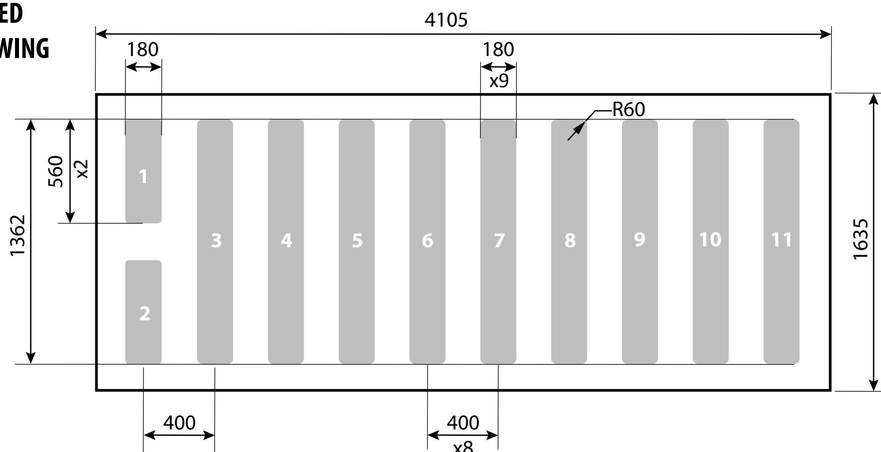
The land pattern is solder mask defined.

Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at https://www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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