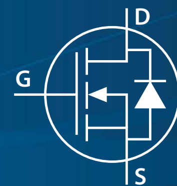
EPC7020 – Rad Hard Power Transistor

V_{DS}, 200 V
$R_{DS(on)}$, 11 mΩ max
I_D, 170 A
95% Pb / 5% Sn Solder

Preliminary



EFFICIENT POWER CONVERSION

Halogen-Free

Rad Hard eGaN® transistors have been specifically designed for critical applications in the high reliability or commercial satellite space environments. GaN transistors offer superior reliability performance in a space environment because there are no minority carriers for single event, and as a wide band semiconductor there is less displacement for protons and neutrons, and additionally there is no oxide to breakdown. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact designs.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150˚C)	240	
I_D	Continuous	39	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	170	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	0.4	°C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	2	
$R_{θJA\_JEDEC}$	Thermal Resistance, Junction to Ambient (using JEDEC 51-2 PCB)	53	
$R_{θJA\_EVB}$	Thermal Resistance, Junction to Ambient (EPC9048C EVB)	26	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.4 mA	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 200 V		10	400	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	0.5	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.1	1.2	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.005	0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A		8	11	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

Defined by design. Not subject to production test.

Die size: 4.6 x 2.6 mm

EPC7020 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

- Space applications: DC-DC power, motor drives, lidar, ion thrusters
- Commercial satellite EPS & avionics
- Deep space probes
- High frequency rad hard DC-DC conversion
- Rad hard motor drives

Features

- Ultra high efficiency
- Ultra low $R_{DS(on)}$, Q_G, Q_{GD} Q_{OSS}, and 0 Q_{RR}
- Ultra small footprint
- Light weight
- Total dose
  - Rated > 1 Mrad
- Single event
  - SEE immunity for LET of 85 MeV/(mg/cm^2) with V_{DS} up to 100% of rated breakdown
- Neutron
  - Maintains pre-rad specification for up to 3 x 10^{15} neutrons/cm^2

Benefits

- Superior radiation and electrical performance vs. rad hard MOSFETs: Smaller, lighter, greater radiation hardness

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC7020

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		1137		pF
C_{RSS}	Reverse Transfer Capacitance			2.6		
C_{OSS}	Output Capacitance			494		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 100 V, V_{GS} = 0 V		592		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			756		
R_G	Gate Resistance			1.3		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 5 V, I_D = 30 A		11.7		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 100 V, I_D = 30 A		3.5		
Q_{GD}	Gate-to-Drain Charge			2.2		
$Q_{G(TH)}$	Gate Charge at Threshold			2.1		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		76		
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
All measurements were done with substrate connected to source.

Figure 1: Typical Output Characteristics at 25°C

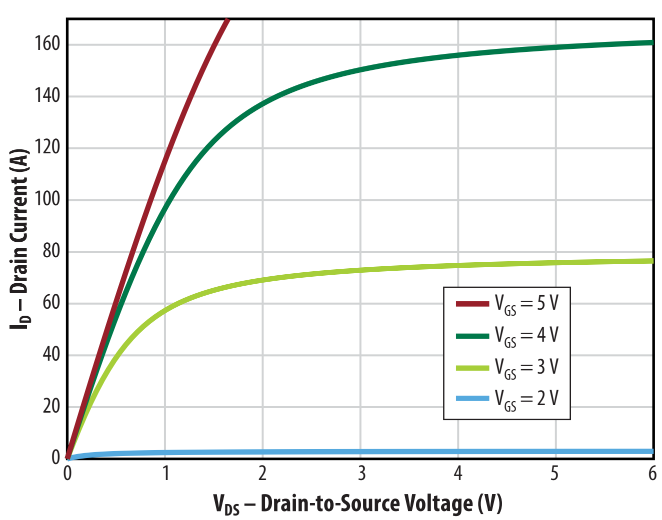


Figure 2: Typical Transfer Characteristics

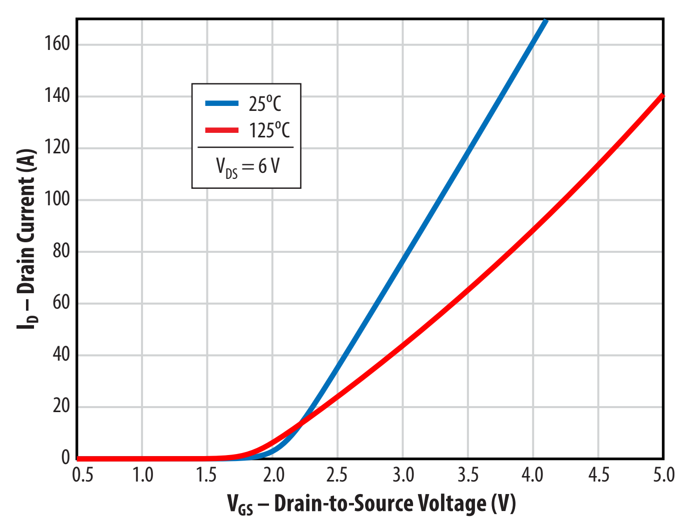


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Currents

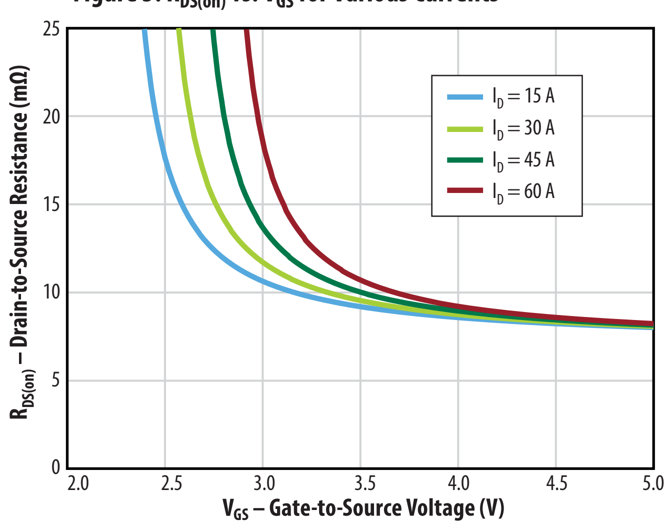


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

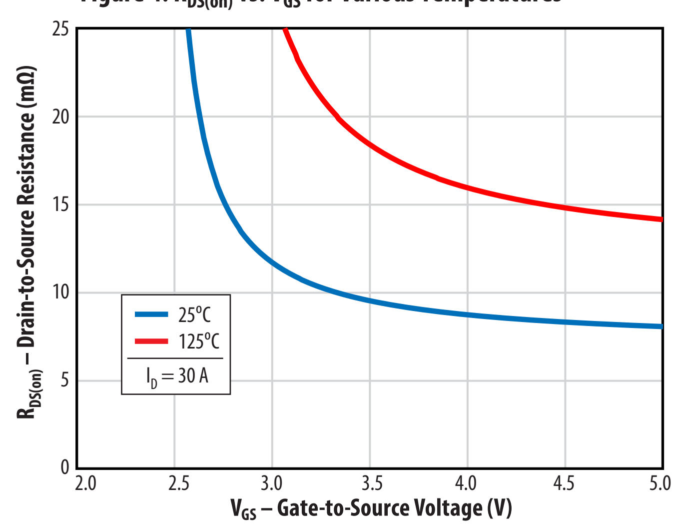


Figure 5a: Typical Capacitance (Linear Scale)

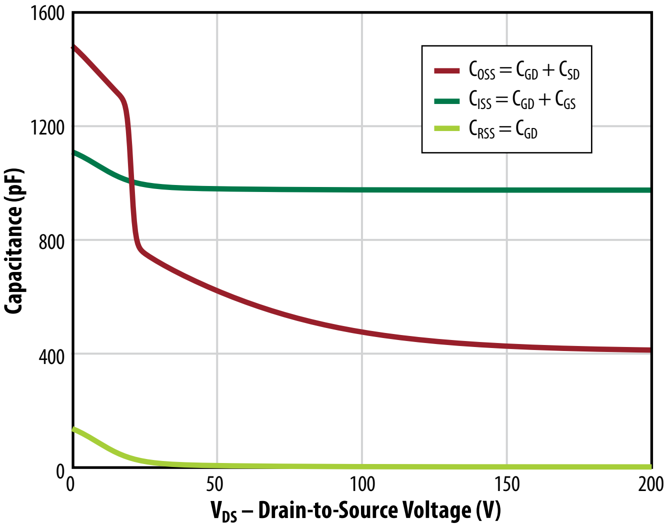


Figure 5b: Typical Capacitance (Log Scale)

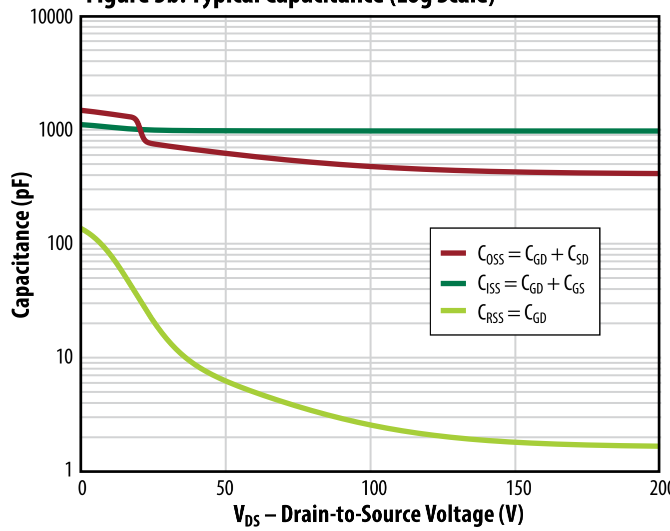


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

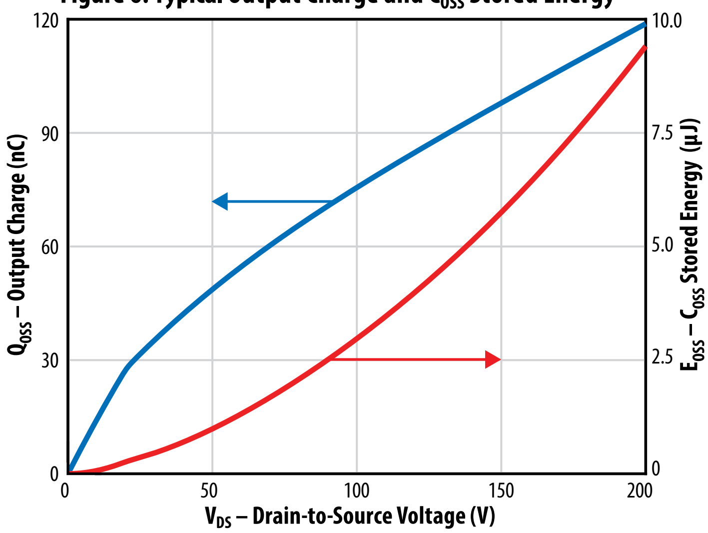


Figure 7: Typical Gate Charge

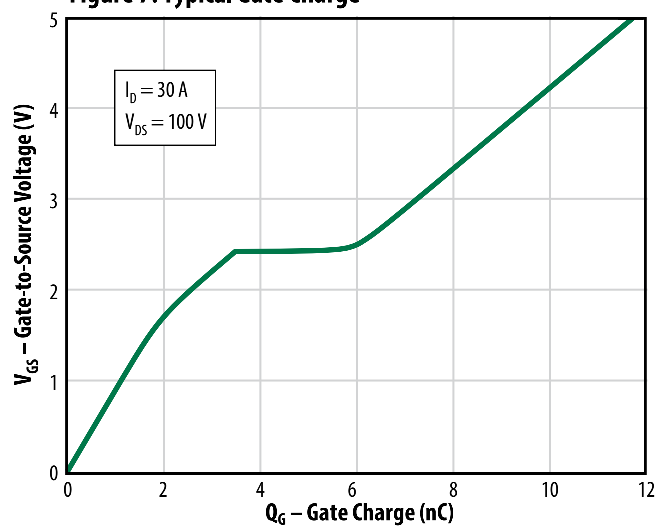
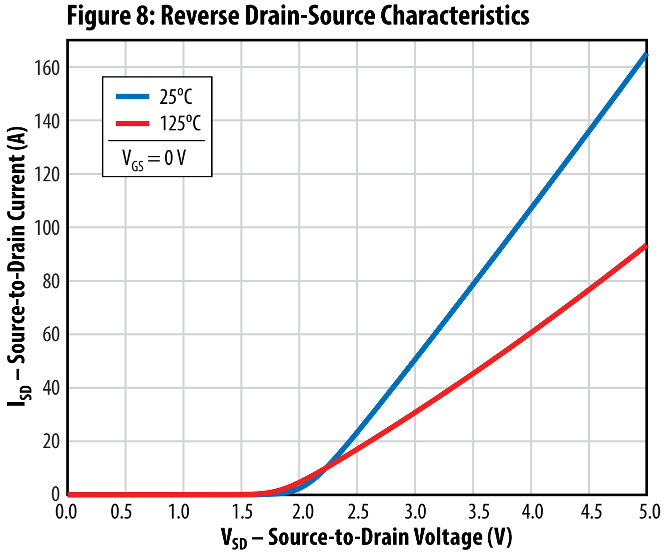


Figure 8: Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Normalized On-State Resistance vs. Temperature

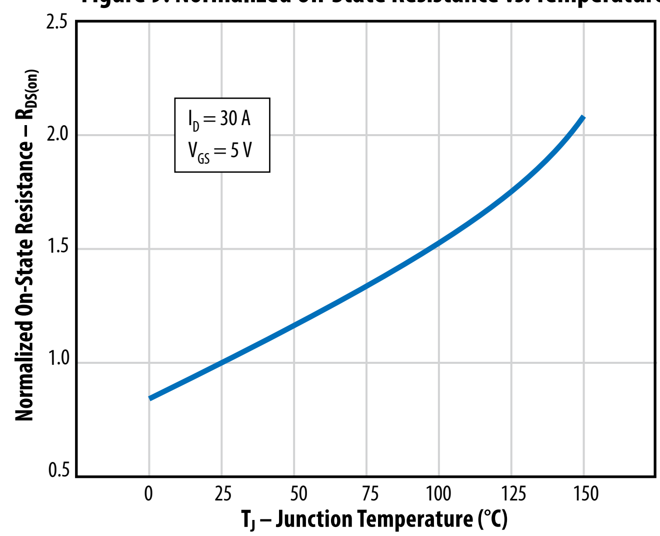


Figure 10: Normalized Threshold Voltage vs. Temperature

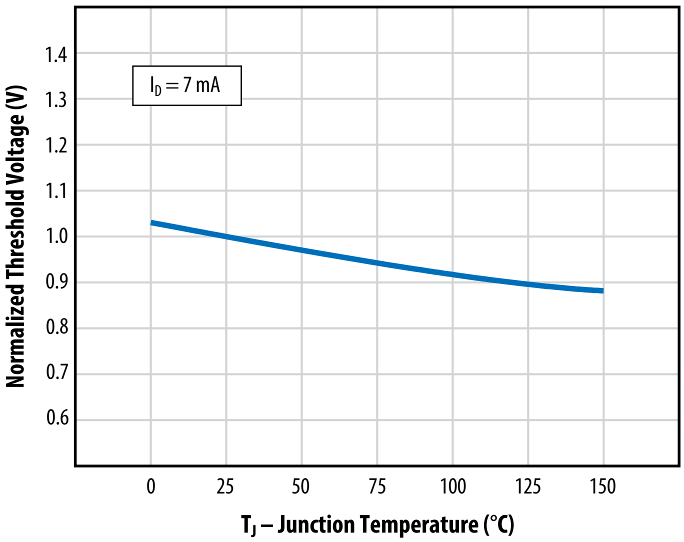


Figure 11: Safe Operating Area

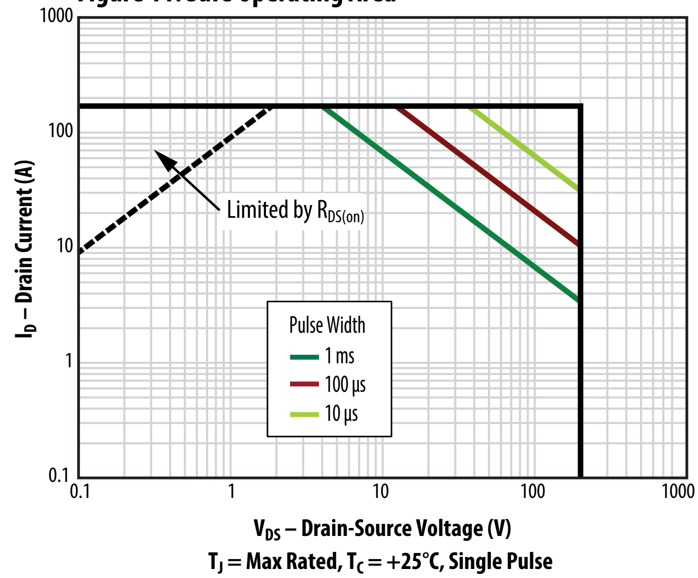
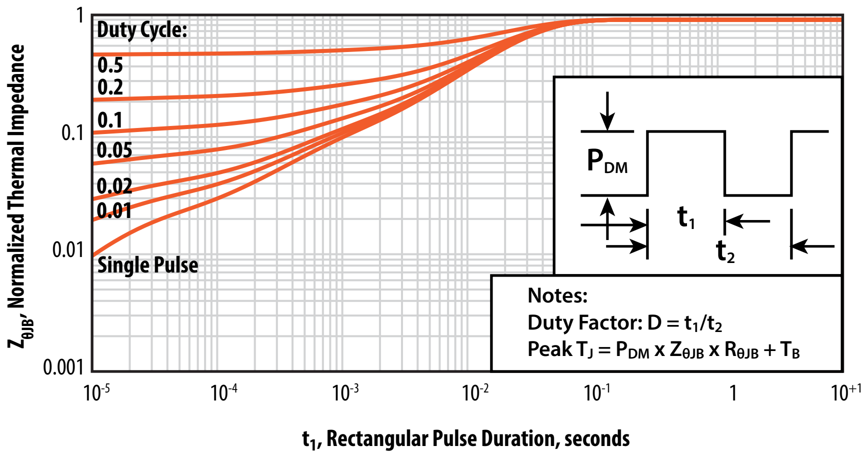
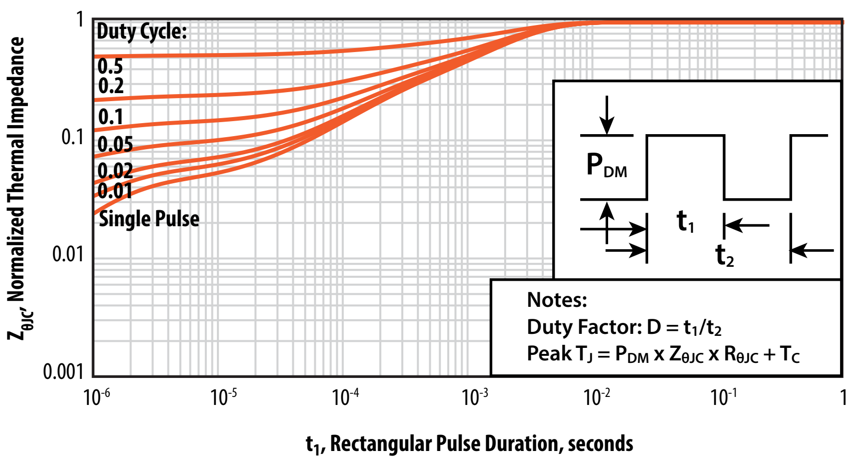


Figure 12: Transient Thermal Response Curves

Junction-to-Board

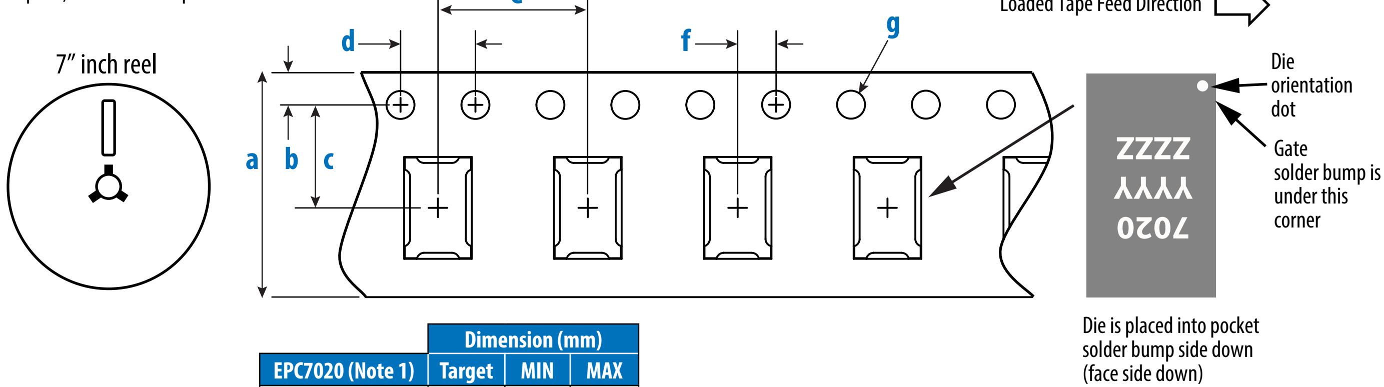


Junction-to-Case



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

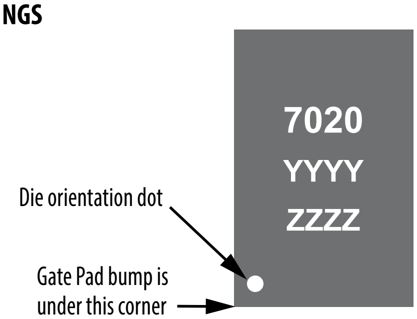


	Dimension (mm)		
EPC7020 (Note 1)	**Target**	**MIN**	**MAX**
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

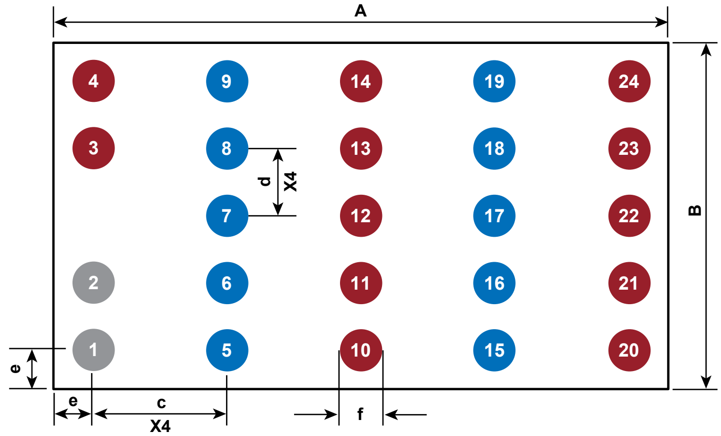
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	**Lot_Date Code Marking Line 2**	**Lot_Date Code Marking Line 3**
EPC7020	7020	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



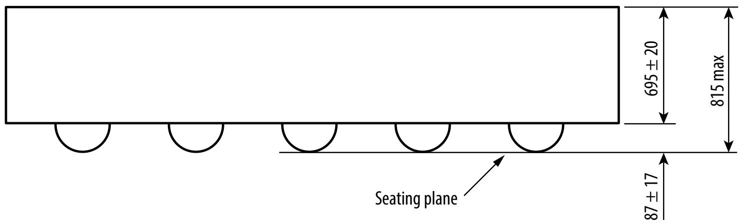
DIM	Micrometers		
	MIN	Nominal	MAX
A	4570	4600	4630
B	2570	2600	2630
c	1000	1000	1000
d	500	500	500
e	285	300	315
f	332	369	406

Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 12, 13, 14, 20, 21, 22, 23, 24 are Source

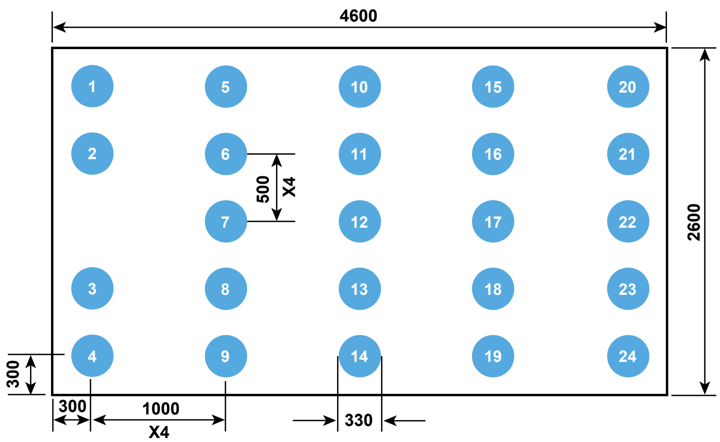
Side View



Note: Substrate (top side) connected to Source

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined

Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 12, 13, 14, 20, 21, 22, 23, 24 are Source

Information subject to change without notice.
Revised February 2023