EPC eGaN® FET Qualification Report EPC2052

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This report summarizes the Product Qualification results for EPC part number EPC2052 which meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification of EPC2045, EPC2051, and EPC2052 listed in the table below. EPC2045, EPC2051, and EPC2052 have the same voltage ratings and device processing.

Part Number	Voltage (V)	$R_{DS(on)}$ (mΩ)	Die Size (mm x mm)
EPC2045	100	7	L (2.5 x 1.5)
EPC2052	100	13.5	M (1.5 x 1.5)
EPC2051	100	25	S (1.3 x 0.85)

Qualification Test Overview

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain source voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts are subjected to a gate source voltage at the maximum rated temperature
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.

The stability of the devices is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) standards when possible.

Parts were mounted onto FR5 (high Tg FR4) or polyimide adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder no clean flux was used in mounting the part onto an adaptor card.

High Temperature Reverse Bias

Parts were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2045	100	L (2.5 x 1.5)	T = 150°C, V_{DS} = 80 V	0	77 x 1	1000
HTRB	EPC2051	100	S (1.3 x 0.85)	T = 150°C, V_{DS} = 80 V	0	77 x 2	1000

Note - EPC2052 is qualified by matrix.

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts were subjected to 5.75 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2045	100	L (2.5 x 1.5)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	1000
HTGB	EPC2051	100	S (1.3 x 0.85)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	1000

Note - EPC2052 is qualified by matrix.

Table 2. High Temperature Gate Bias Test

High Temperature Storage

Parts were subjected to heat at the maximum rated temperature.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2045	100	L (2.5 x 1.5)	T = 150°C, Air	0	77 x 2	1000
HTS	EPC2051	100	S (1.3 x 0.85)	T = 150°C, Air	0	77 x 4	1000

Note - EPC2052 is qualified by matrix.

Table 3. High Temperature Storage Test

Temperature Cycling

Parts were subjected to temperature cycling between -40°C and +125°C, with a ramp rate of 15°C/min and dwell time of 5 minutes in accordance with the JEDEC Standard JESD22A104.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2045	100	L (2.5 x 1.5)	-40 to +125°C, Air	0	77 x 3	1000
TC	EPC2051	100	S (1.3 x 0.85)	-40 to +125°C, Air	0	77 x 3	500*

***Note** - EPC2051 is supplied in passivated die form with copper pillars. EPC2052 is qualified by matrix.
Customers will qualify the die in their products themselves.
The 500 cycle TC data is for reference only.

Table 4. Temperature Cycling Test

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias at 85% RH and 85°C for a stress period of 500 or 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22A101.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2045	100	L (2.5 x 1.5)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	77 x 1	500
H3TRB	EPC2051	100	S (1.3 x 0.85)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	77 x 2	1000

Note - EPC2052 is qualified by matrix.

Table 5. High Temperature High Humidity Reverse Bias Test

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC2051	100	S (1.3 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	77 x 3	168

Note - EPC2052 is qualified by matrix.

Table 6. Moisture Sensitivity Level Test